RAMA UNIVERSITY

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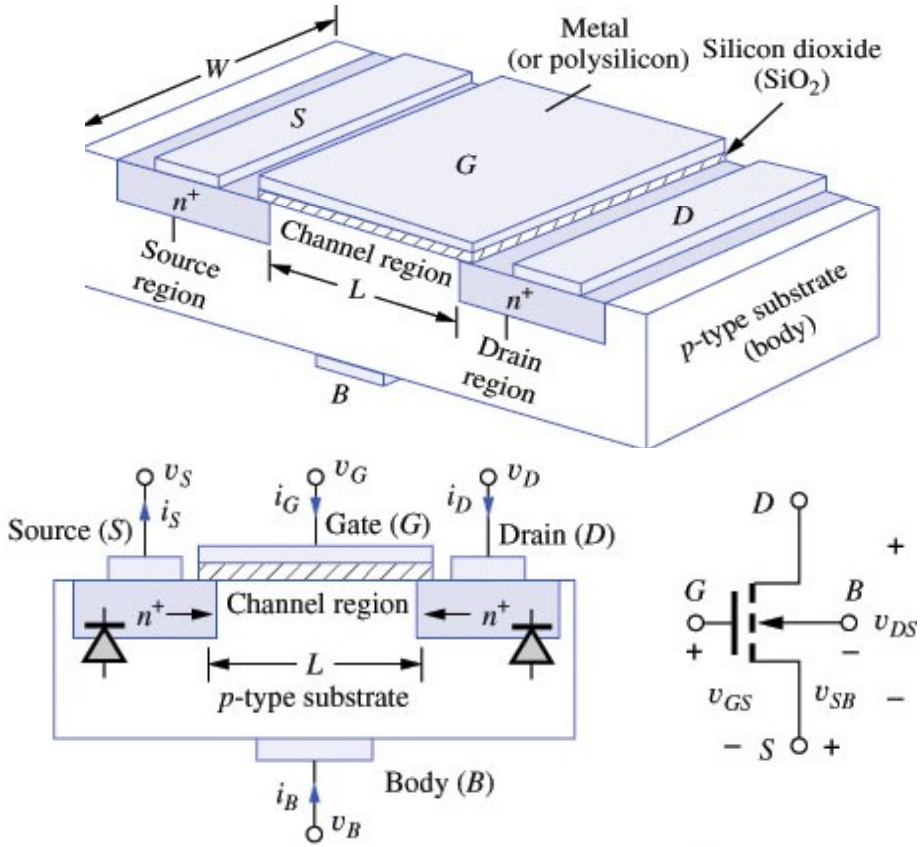
FACULTY OF ENGINEERING AND TECHNOLOGY

MEC-022

Lecture - 05

NMOS Transistor: Structure

A N-MOSFET is formed by adding two heavily doped *n*-type (n^+ , about one of 100 of silicon atoms is replaced with donor), regions to the MOS capacitor. The resulting diffusions provide a supply of electrons that can rapidly form the inversion layer and easily move under the gate, and also make terminals to apply a voltage and create a current in the channel region.



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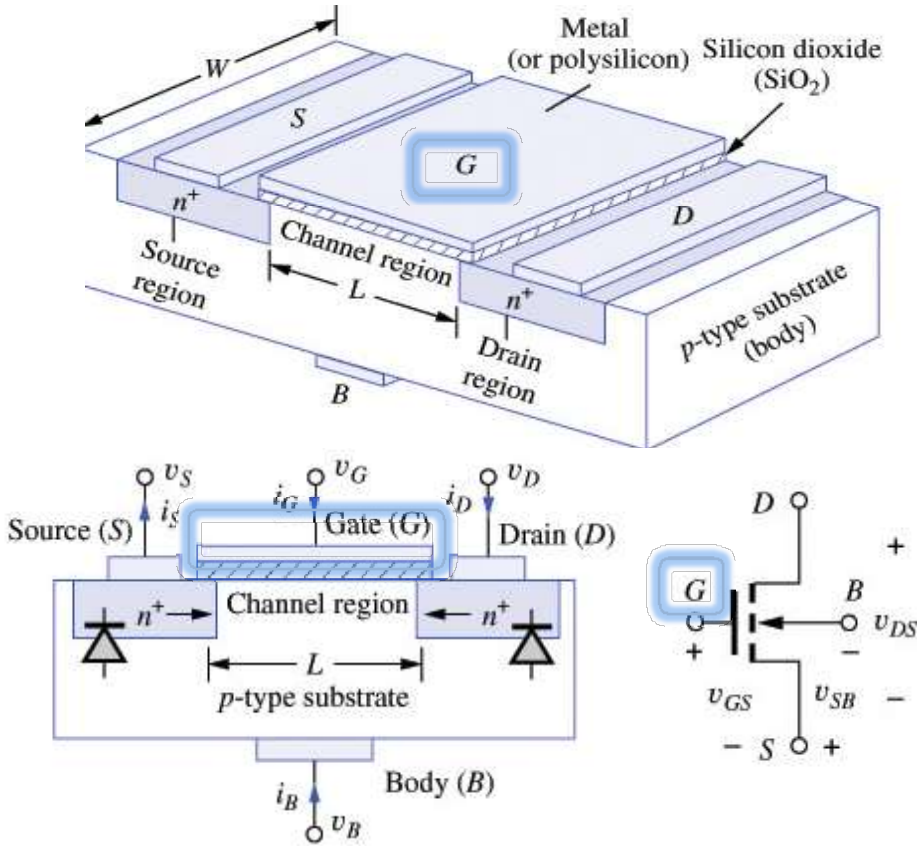

- 4 device terminals:

  Gate(G)

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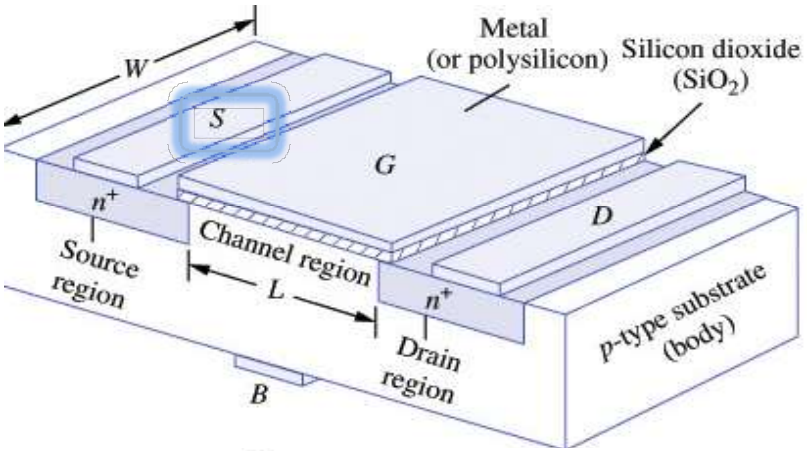

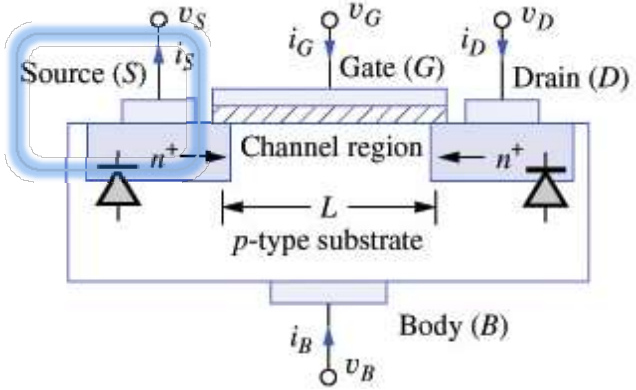

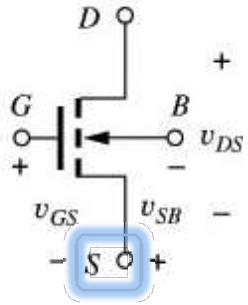

- 4 device terminals:
  - Gate(G)
  - Drain(D),
  - Source(S)

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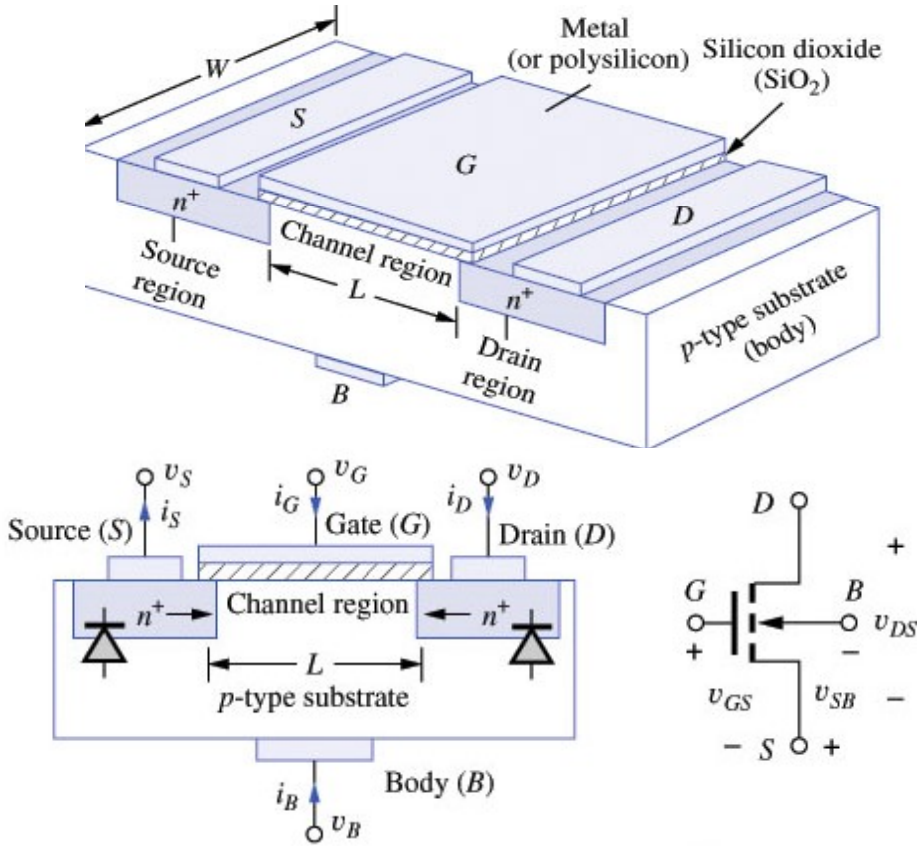
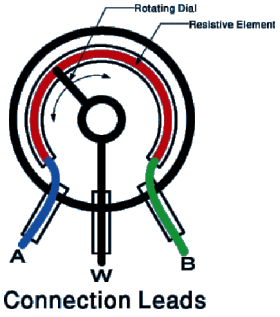
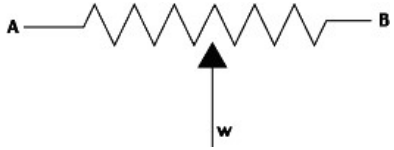


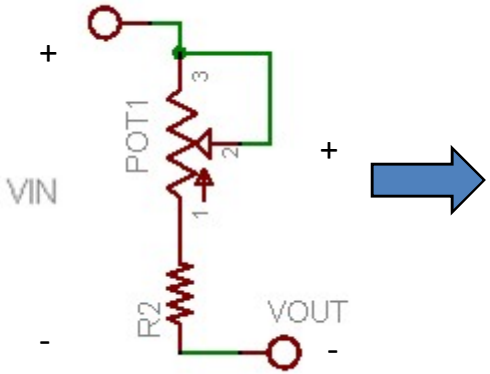
- 4 device terminals:
  - Gate(G)
  - Drain(D),
  - Source(S)
  - Body(B).
- Source and drain regions form *pn* junctions with substrate.
- $v_{SB} = v_S - v_B$, $v_{DS} = v_D - v_S$ and $v_{GS} = v_G - v_S$ are always positive during normal operation.
- $v_B <= v_D$ and $v_B <= v_S$, to keep *pn* junctions reverse biased.

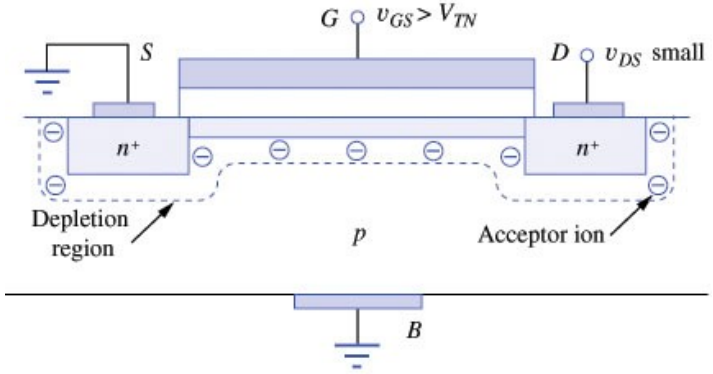
NMOS Transistor and Variable Resistor



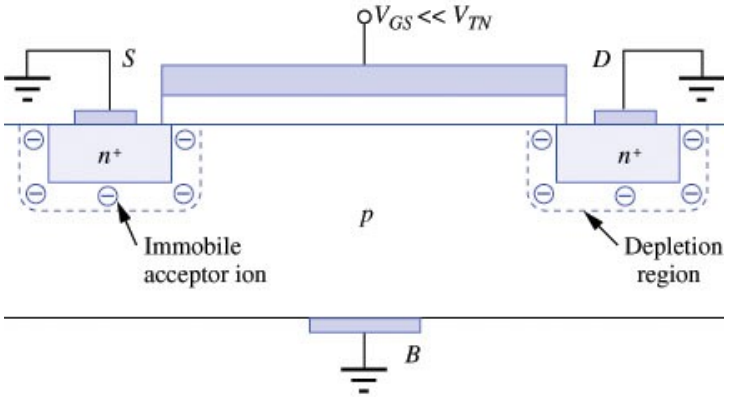
- A transistor is a three (or four) terminal device, in which one terminal controls the voltage or current between other two terminals
- In certain way it is similar to a variable resistor, in which the movement of the middle terminal controls the voltage.







NMOS Transistor: Qualitative Behavior @ v_{DS} =0



- $V_{GS}<<V_{TN}$ ($V_{GS}<0$): Two back to back reverse biased *pn* junctions btw S and D. Only small leakage current flows.


Thank You!