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FACULTY OF ENGINEERING & TECHNOLOGY

CSPS-106 Computer Organization

Lecture-09

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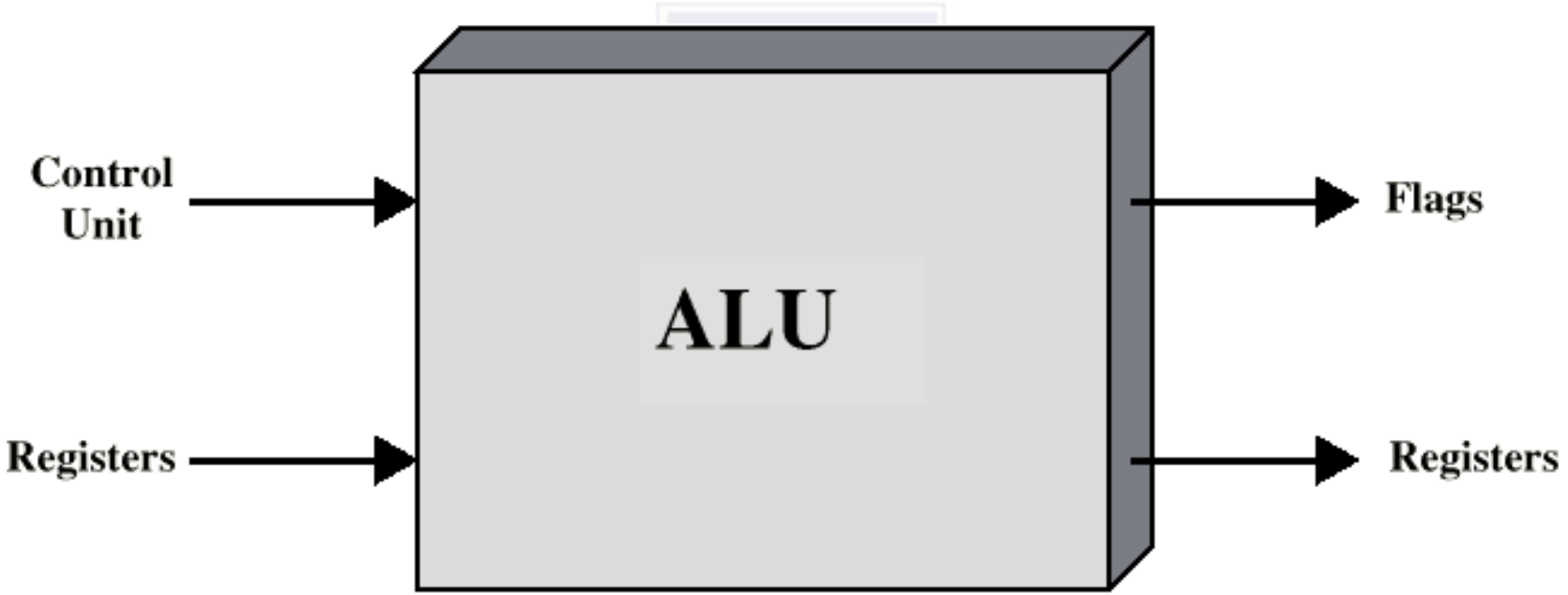
OUTLINE

- ARITHMETIC & LOGIC UNIT
- ALU INPUTS AND OUTPUTS
- INTEGER REPRESENTATION
- SIGN-MAGNITUDE
- GEOMETRIC DEPICTION OF TWOS COMPLEMENT INTEGERS
- NEGATION SPECIAL CASE

ARITHMETIC & LOGIC UNIT

- Does the calculations
- Everything else in the computer is there to service this unit
- Handles integers
- May handle floating point (real) numbers
- May be separate FPU (maths co-processor)
- May be on chip separate FPU (486DX +)

ALU INPUTS AND OUTPUTS



INTEGER REPRESENTATION

- Only have 0 & 1 to represent everything
- Positive numbers stored in binary
  - e.g. 41=00101001
- No minus sign
- No period
- Sign-Magnitude
- Two’s compliment

SIGN-MAGNITUDE

- Left most bit is sign bit
- 0 means positive
- 1 means negative
- +18 = 00010010
- -18 = 10010010
- Problems
  - Need to consider both sign and magnitude in arithmetic
  - Two representations of zero (+0 and -0)

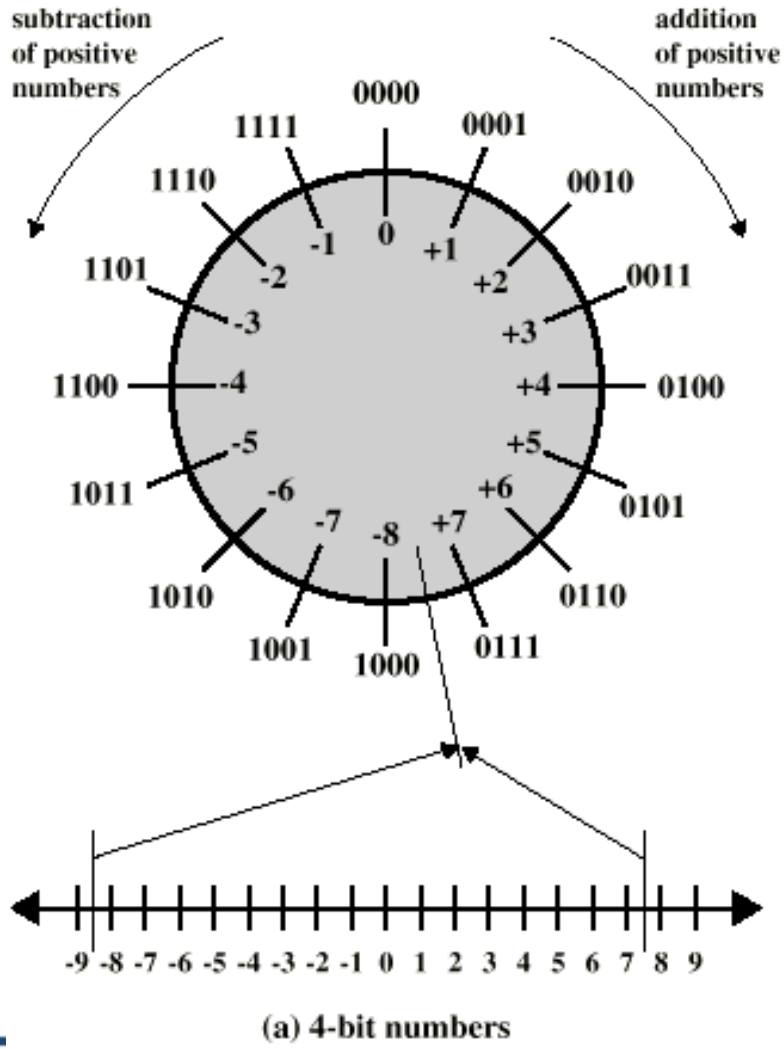
TWO'S COMPLIMENT

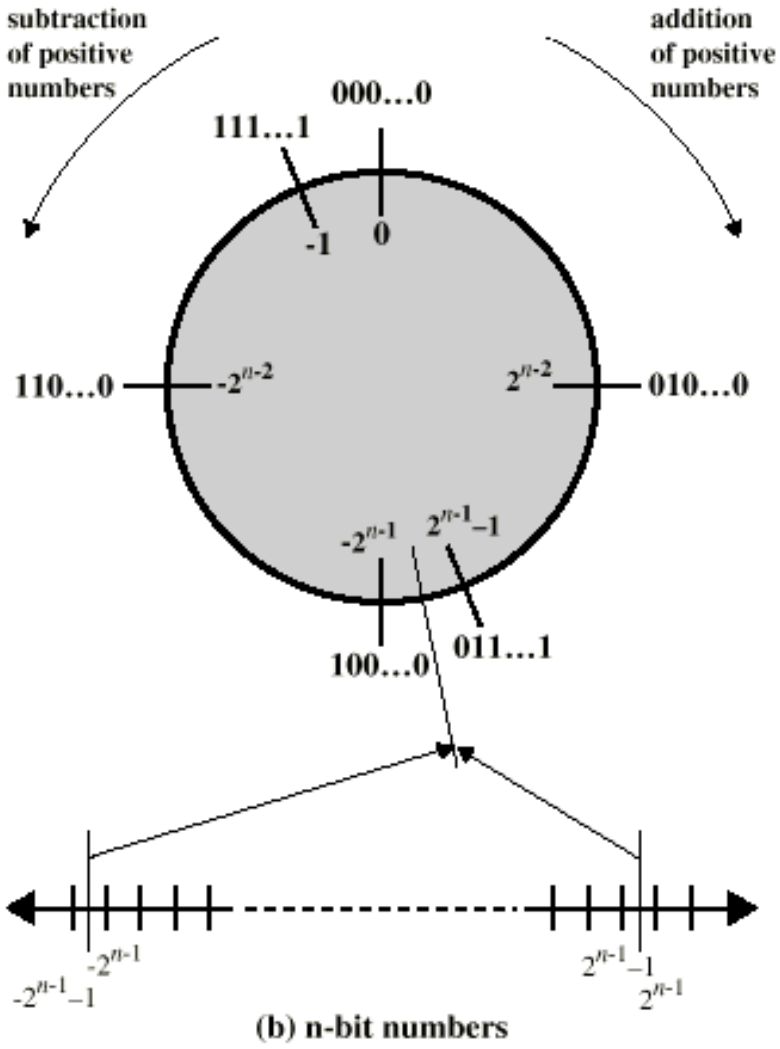
- +3 = 00000011
- +2 = 00000010
- +1 = 00000001
- +0 = 00000000
- -1 = 11111111
- -2 = 11111110
- -3 = 11111101

BENEFITS

- One representation of zero
- Arithmetic works easily (see later)
- Negating is fairly easy
  - 3 = 00000011
  - Boolean complement gives 11111100
  - Add 1 to LSB 11111101

GEOMETRIC DEPICTION OF TWOS COMPLEMENT INTEGERS





NEGATION SPECIAL CASE 1

- 0 = 00000000
- Bitwise not 11111111
- Add 1 to LSB +1
- Result 1 00000000
- Overflow is ignored, so:
- - 0 = 0 √

NEGATION SPECIAL CASE 2

- -128 = 10000000
- bitwise not 01111111
- Add 1 to LSB +1
- Result 10000000
- So:
- -(-128) = -128 X
- Monitor MSB (sign bit)
- It should change during negation

Multiple Choice Question

MUTIPLE CHOICE QUESTIONS:

Sr no	Question	Option A	Option B	OptionC	OptionD
1	For the addition of large integers, most of the systems make use of _____	Fast adders	Full adders	Carry look-ahead adders	None of the mentioned
2	In a normal n-bit adder, to find out if an overflow as occurred we make use of _____	And gate	Nand gate	Nor gate	Xor gate
3	In the implementation of a Multiplier circuit in the system we make use of _____	Counter	Flip flop	Shift register	Push down stack
4	When 1101 is used to divide 100010010 the remainder is _____	11	10	1	1
5	Which error detection arithmetic?	Simple parity check	Two-dimensional parity check	CRC	Checksum

REFERENCES

- http://www.engppt.com/search/label/Computer%20Organization%20and%20Architecture
- http://www.engppt.com/search/label/Computer%20Architecture%20ppt