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FACULTY OF ENGINEERING & TECHNOLOGY

CSPS-106 Computer Organization

Lecture-10

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OUTLINE

- RANGE OF NUMBERS
- ADDITION AND SUBTRACTION
- MULTIPLICATION
- UNSIGNED BINARY MULTIPLICATION

RANGE OF NUMBERS

- 8 bit 2s compliment
  - +127 = 01111111 = 2^7 -1
  - -128 = 10000000 = -2^7
- 16 bit 2s compliment
  - +32767 = 011111111 11111111 = 2^{15} - 1
  - -32768 = 100000000 00000000 = -2^{15}

CONVERSION BETWEEN LENGTHS

- Positive number pack with leading zeros
- +18 = 00010010
- +18 = 00000000 00010010
- Negative numbers pack with leading ones
- -18 = 10010010
- -18 = 11111111 10010010
- i.e. pack with MSB (sign bit)

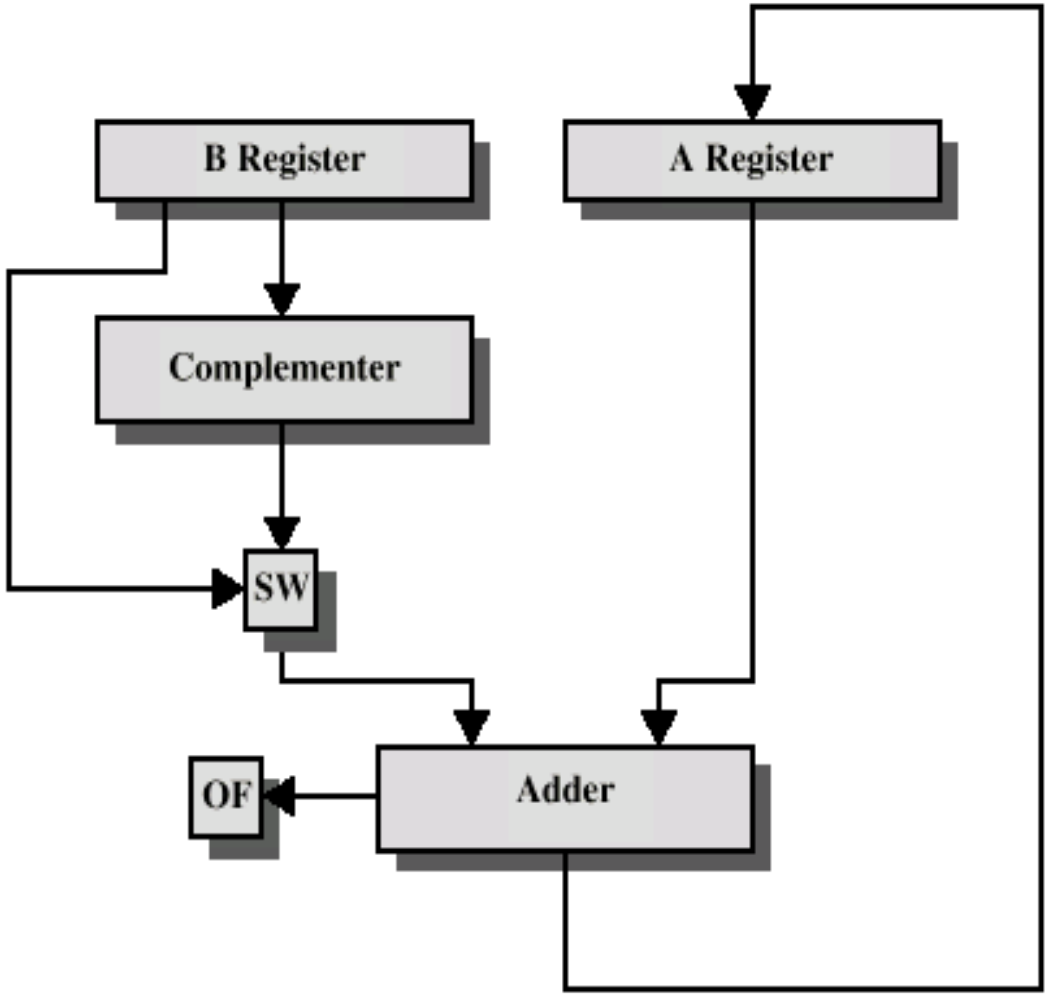
ADDITION AND SUBTRACTION

- Normal binary addition
- Monitor sign bit for overflow

- Take twos compliment of substahend and add to minuend
  - i.e. a - b = a + (-b)

- So we only need addition and complement circuits

Hardware for Addition and Subtraction

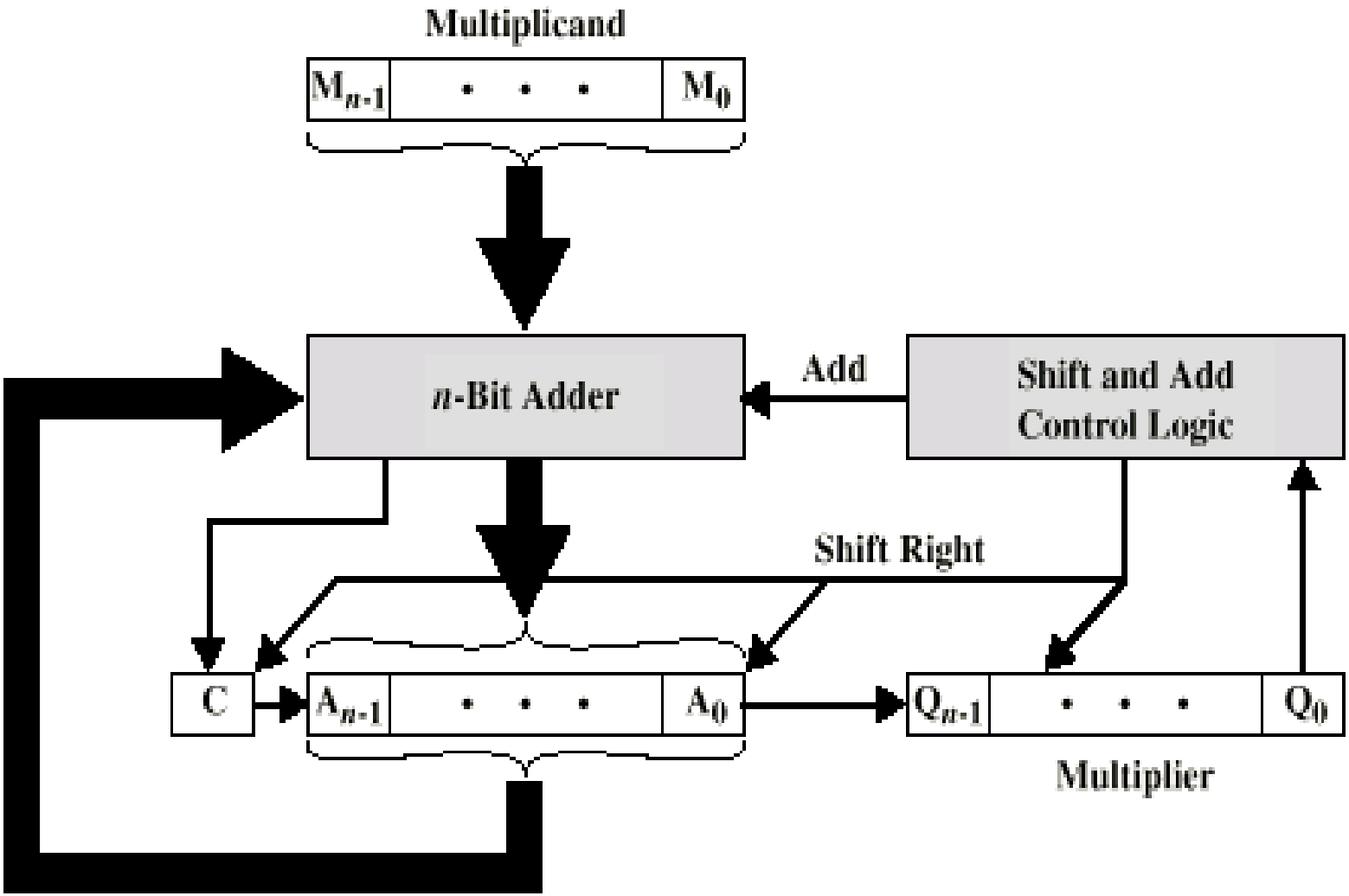


OF = overflow bit
SW = Switch (select addition or subtraction)

MULTIPLICATION

- Complex
- Work out partial product for each digit
- Take care with place value (column)
- Add partial products
- 1011 Multiplicand (11 dec)
- x 1101 Multiplier (13 dec)
- 1011 Partial products
- 0000 Note: if multiplier bit is 1 copy
- 1011 multiplicand (place value)
- 1011 otherwise zero
- 10001111 Product (143 dec)
- Note: need double length result

UNSIGNED BINARY MULTIPLICATION

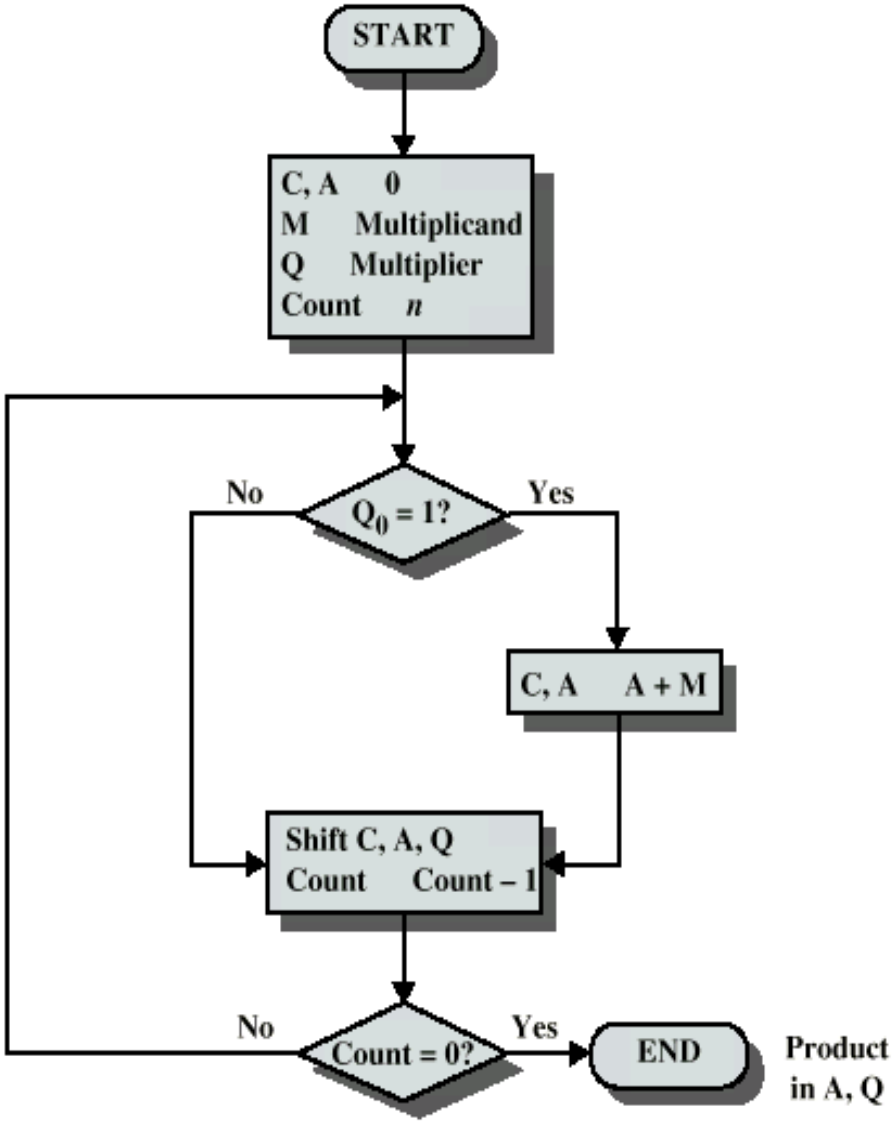


(a) Block Diagram

EXECUTION OF EXAMPLE

C	A	Q	M		
0	0000	1101	1011	Initial Values	
0	1011	1101	1011	Add	First Cycle
0	0101	1110	1011	Shift	
0	0010	1111	1011	Shift	Second Cycle
0	1101	1111	1011	Add	Third Cycle
0	0110	1111	1011	Shift	
1	0001	1111	1011	Add	Fourth Cycle
0	1000	1111	1011	Shift	

FLOWCHART FOR UNSIGNED BINARY MULTIPLICATION



MULTIPLYING NEGATIVE NUMBERS

- This does not work!
- Solution 1
  - Convert to positive if required
  - Multiply as above
  - If signs were different, negate answer
- Solution 2
  - Booth's algorithm

Multiple Choice Question

MUTIPLE CHOICE QUESTIONS:

Sr no	Question	Option A	Option B	OptionC	OptionD
1	Which error detection redundant bit per day unit	Simple parity check	Two-dimensional parity check	CRC	Checksum
2	In cyclic redundancy checking, what is the crc	The divisor	The quotient	The dividend	The remainder
3	In cyclic redundancy checking, thedivisoris the CRC	The same size as	one bit less than	one bit more than	none of theabove
4	burst error means that two or more bits in the dataunit havechanged.	double-bit	burst	single-bit	none of theabove
5	error correction, the receiver corrects errors without requesting retransmission.	backward	onward	forward	none of the above

REFERENCES

- http://www.engppt.com/search/label/Computer%20Organization%20and%20Architecture
- http://www.engppt.com/search/label/Computer%20Architecture%20ppt