Ref: RU/FET/EE/BOS/2020/002

Dated: 20/04/2020

Faculty of Engineering & Technology

Department of Electronic & Communication Engineering

Minutes of Meeting

Boards of Studies

A meeting of Boards of Studies of Electronic & Communication Engineering, FET was held on 20/04/2020 (Monday) at 2:30 PM. in conference room of FET. The following members were present:

1. Mr.Samir Kumar Mishra - Chairperson
3. Ms.Raghvendra Singh - Member
3. Mr. Dileep Kumar - Member

The following members agreed to review the minutes in Delhi.

1. Prof. Shyam Akashe - External Member
2. Dr. Sunil Kumar Panday - External Member

In view of the existing pandemic of Covid-19, all social distancing norms were observed. The External Expert, Dr. Vishal Awasthi agreed to join the proceedings online via Zoom app.

Agenda:

1. **Action Taken Report (ATR) on the basis of feedback from Stack holder/External member**

   The department teams have been working on the curricula and syllabus and consider their feedback and suggestion of stack holder/External member. They suggested that the focus must be on fundamental and practical courses having emphasis on research and development.

   Action taken: Courses like (i) Semiconductor of Device Modeling (ii) Architectural Design of ICs (iii) Digital VLSI Circuit (iv) Nano Technology.

2. **To review the Vision and Mission statements of the newly established of Electronics & Communication Engineering Department.**

   The Board of Studies reviewed the Vision and Mission statements prepared by the HoD, ECE. The Board suggested minor revisions in the both the statements and recommends the final draft for adoption by the Academic Council.

Attached revised Vision and Mission statements in Annexure: 1.

3. **To review the Program Outcomes (PO), Program Specific Outcomes (PSO) and Program Educational Objectives (PEO) for M.Tech program (Part Time).**

The Board reviewed the Program Outcomes (POs) for M.Tech. Program and revised them to fit into the Frame work laid down by the National Board of Accreditation.

The Program Specific Outcomes (PSO) and Program Educational Objectives (PEO) for M.Tech. Program (Part Time) were reviewed and recommended for approval by the Academic Council.

(Annexure 2 & 3)

4. **To consider and approved the curricula and syllabus.**

S. No.	Item No.	Existing	Recommendation /Action Taken
1	To conceder and recommendation the evaluation scheme & syllabus for M.Tech(Part Time). students admitted in the session 2020-21.	....	The BOS consider the curricula and syllabus and discuss the credit of each subjects should be added in detailed syllabus of every subject. The BOS recommended the curricula and syllabus for approval by the Academic Council. The BOS discussed the item and Recommended for approval the revised syllabus of P.G Course Electronic & Communication Engineering which is designed as per CBCS system. **(Annexure 4)**

The meeting concluded with a vote of thanks to the chair.

Date of the Next Meeting: to be decided and conveyed later

(Chairman)

CC:
1. Dean
2. Registrar Office

RAMA UNIVERSITY, UTTAR PRADESH, KANPUR
FACULTY OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Website: www.ramauniversity.ac.in

ACADEMIC REGULATIONS 2020-21

(As per AICTE Model Curriculum)

For CBCS Based M.Tech. (Part Time) Programmes

1.0 Post-Graduate Degree Programmes in Engineering & Technology (PGP in E&T):

Department of Electronics & Communication Engineering, Faculty of Engineering & Technology offer three-year (Six Semesters) Part-Time Master of Technology (M.Tech.) Degree Programmes, under Choice Based Credit System (CBCS) with effect from the Academic Year 2020-21 and onwards in the following specializations:
(1) Microelectronics &VLSI Design

Eligibility for Admission:

Admissions to the Post Graduate Programmes in Department of Electronics & Communication Engineering shall be made subject to the eligibility, qualification and specializations prescribed by Rama University Uttar Pradesh from time to time, for each Specialization under each M.Tech.Programme.

Admission to the Post Graduate Programmes in Department of Electronics & Communication Engineering shall be made either on the basis of the qualifying student at an Entrance Test conducted by the Rama University Uttar Pradesh, Kanpur, subject to reservations as prescribed by the Government from time to time.

The medium of instructions for all Post Graduate Programmes will be ENGLISH only.

M.Tech. Programme (Department of Electronics & Communication Engineering, Faculty of Engineering & Technology) Structure:

The M.Tech. Programmes in Department of Electronics & Communication Engineering, Faculty of Engineering & Technology are of Semester Pattern,

1. For Part Time Programme, with 6 Semesters constituting 3 Academic Years,

   Each Academic Year having TWO Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 Weeks duration (inclusive of Examinations), with a minimum of 90 Instructional Days per Semester.

UGC/ AICTE specified Definitions/ Descriptions are adopted appropriately for various terms and abbreviations used in these PGP - Academic Regulations, as listed below.

Semester Scheme:

Each Semester having - 'Continuous Assessment (CA)' and 'Mid-Semester Examination (MTE)' 'Semester End Examination (ETE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as denoted are taken as 'references' for the present set of Regulations. The terms 'Subject' or 'Course' imply the same meaning here, and refer to 'Theory Subject', or 'Practical Subject', or 'Seminar', 'Dissertation', as the case maybe.

Credit Courses:

All Subjects (or Courses) are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Subject/ Course in a L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) Structure, based on the following general pattern…

- One credit for One hour/ Week/ Semester for Theory/ Lecture (L) or Tutorial (T)Courses;

- One credit for Two hours/ Week/ Semester for Laboratory/ Practical (P) Courses.
- Other student activities like Study Tour, Guest Lecture, Conference/ Workshop Participations, Technical Paper Presentations etc., and identified Audit Courses if any, will not carry Credits.

Subject/ Course Classification:

The Department of Electronics & Communication Engineering, Faculty of Engineering & Technology has followed the guidelines issued by AICTE/UGC. All Subjects/Courses offered for the Post Graduate Programmes in Department of Electronics & Communication Engineering, Faculty of Engineering & Technology are broadly classified as Program Core, Program Elective, Seminar and Dissertation.

Course Nomenclature:

The Curriculum Nomenclature or Course-Structure Grouping for the M.Tech. Degree Programmes is as listed below …

S. No.	Broad Course Classification	Course Group/ Category	Courses Description
1	Core Courses	PC- Program Core	Includes core subjects related to the Parent Discipline/ Department/ Branch of Engineering
		Dissertation	M.Tech. Project
		Seminar	Seminar based on core contents related to parent discipline/department/branch of Engineering
2	Elective Courses	PE– Program Electives	Includes Elective subjects related to the Parent Discipline/ Department/ Branch of Engineering
3	Open Elective Courses	OE– Open Electives	Includes Elective subjects related to the Parent Discipline/ Department/ Branch of Engineering

Course Work:

A Student, after securing admission, shall pursue and complete the M.Tech. Post Graduate Programmes in Department of Electronics & Communication Engineering, Faculty of Engineering & Technology

1. in a minimum period of Three-Academic Years (Six Semesters), and within a maximum period of Five-Academic Years (Ten Semesters) starting from the Date of Commencement of I Year / I Semester for Part Time Programme.

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ACADEMIC REGULATIONS 2020-21

(As per AICTE Model Curriculum)

For CBCS Based M.Tech. (Part Time) Programmes

Each student shall register for and secure the specified number of Credits required for the completion of the Post Graduate Programme and Award of the M.Tech. Degree in Electronics & Communication Engineering with the chosen Specialization.

1. All Years are structured to provide typically 16 Credits in each of the Semesters in I year, 10 and 11 credits in each of the Semesters in II year and V Semester in III year, 11 and 16 credits in V and VI Semester of III year totaling to 80 Credits for the entire M.Tech. Programme, (Part Time).

Course Registration:

A 'Faculty Mentor' shall be assigned to each M.Tech. Programme with respective Specialization, who will mentor the Students about the M.Tech. Programme Specialization, its Course Structure and Curriculum, Choice/ Option for Subjects/ Courses, based on the competence, progress, pre-requisites and interest of thestudents.

A Student, in case of Part Time Course may be permitted to Register for Subjects/ Courses of 'his Choice' with a total of 12 and 10 Credits per Semester in I and II year respectively and III Year (Minimum being 10and 8 Credits and Maximum being 14 and 12 Credits respectively) and with a total credit of 10 and 16 in the Semester V and VI respectively of III year (Minimum being 8 and 14 Credits and Maximum being 12 and 18 Credits respectively), based on his interest, competence, progress, and 'Pre-requisites' as indicated for various Subjects/ Courses, in the Department Course Structure (for the relevant Specialization) and Syllabus contents for various Subjects/ Courses.

Choice for 'additional Subjects/ Courses' in any Semester (above the typical Credit norm, and within the Maximum Permissible, complete Years as applicable) must be clearly indicated in the Registration, which needs the specific approval and signature of the Faculty Mentor/ Counselor on hard-copy.

Withdraw of Subjects/ Courses in any Semester of I Year may be permitted, ONLY AFTER obtaining prior approval and signature from the Faculty Mentor (subject to retaining a minimum Credits), 'within 15 Days of Time' from the beginning of the current Semester.

Attendance Requirements:

A Student shall be eligible to appear for the Semester End Examination (ETE) of any Subject, if he acquires a minimum of 75% of attendance in class work in that Subject for that Semester.

Condoning of shortage of attendance up to 10% (65% and above, and below 75%) in each Subject of a Semester may be granted by the University Academic Council on Medical grounds, based on the Student's representation with supporting evidence to be submitted by the student as and when such requirement arise but not at the end semester.

A stipulated fee per Subject, shall be payable towards condoning of shortage of attendance after getting the approval of University Academic Council for the same.

Shortage of Attendance below 65% in any Subject shall in NO case be condoned.

A Student, whose shortage of attendance is not condoned in any Subject(s) , is considered as 'Detained in that Subject(s)', and is not eligible to write Semester End Examination(s) of such Subject(s) and are not eligible for evaluation in that Semester; and he has to seek Re-registration for those Subject(s), in subsequent Semesters, and attend the same as and

when offered.

A student fulfilling the attendance requirement in the present semester shall not be eligible for readmission into the same class.

Academic Requirements:

The following Academic Requirements have to be satisfied, in addition to the attendance, the performance of the student in each semester shall be evaluated subject – wise,

1. with a maximum of 150 marks per subject / course (theory), on the basis of Continuous Assessment, Mid-Term and Semester End Examination
2. With a maximum of 50 marks per subject / course (Lab),on the basis of Continuous Assessment and Semester End Examination.
3. With a maximum of 300 marks and 800 marks for Dissertation-I, Dissertation-I and Dissertation-III respectively, on the basis of Continuous Assessment and Semester End Examination.

A Student shall be deemed to have satisfied the academic requirements and earned the Credits allotted to each Subject/ Course

1. (Theory), if he secures not less than 40% Marks in the Semester End Examination, and a minimum of 50% of marks in the sum total of the Internal assessment (Continuous Assessment and Mid-Term Examination) and Semester End Examination taken together;
2. (Lab, Dissertation-I, II& III), if he secures not less than 50% Marks in the Semester End Examination, and a minimum of 60% of marks in the sum total of the Internal assessment (Continuous Assessment) and Semester End Examination taken together;

A Student shall be deemed to have satisfied the academic requirements and earned the Credits allotted to - Seminar, if he secures not less than 50% of the total 100 Marks to be awarded. The Student would be treated as failed, if he-
(i) does not present the Seminar as required, or
(ii) Secures less than 50% of Marks (< 50 Marks) in Seminar.

A Student shall - register for all Subjects covering 80 Credits and 72 credits for Full time and Part Time Course respectively as specified and listed in the Course Structure for the chosen Post Graduate Programme Specialization, put up all the Attendance and Academic requirements for securing full Credits

Students who fail to earn full Credits as per the specified Course Structure, and as indicated above, within Four and Six academic years respectively for Full time and Part Time Course respectively from the date of commencement of their I Year I Semester, shall forfeit their seats in M.Tech. Programme and their admissions shall stand cancelled.

When a Student is detained due to shortage of attendance in any Subject(s) in any Semester, credit Allotment will be considered for such Subject(s) and will not include the performance evaluations of such Subject(s) in which he got detained. However, he becomes eligible for re-registration of such Subject / in the subsequent Semester(s), as and when next offered, with the Academic Regulations of the Batch into which he /she gets re-registered , by paying the stipulated fees per Subject. In all these re-registration cases, the Student shall have

to secure a fresh set of Internal Marks and Semester End Examination Marks for performance evaluation in such Subject(s) to earn stipulated credits.

A Student eligible to appear in the Semester End Examination in any Subject, but absent at it or failed , may reappear for that Subject at the supplementary examination (SEE) as and when conducted. In such cases, his Internal Marks assessed earlier for that Subject/ Course will be carried over, and added to the marks to be obtained in the supplementary examination , for evaluating his performance in that Subject.

Evaluation - Distribution and weight age of Marks:

The performance of a Student in each Semester shall be evaluated Subject-wise (irrespective of Credits assigned) with a maximum Marks for Theory or Practical's or Seminar or Dissertation-I, Dissertation-II &Dissertation-II.

a) For Theory Subjects, during the Semester, there shall be2mid-term examinations of 20 marks (with a duration of 60 minutes each). Further, there will be an allocation of 30 marks for Assignment, Attendance and General Proficiency.

b) The first mid-term examination shall be conducted for the first 2 units of the syllabus, and the second mid-term examination shall be conducted for the remaining units of the syllabus.

c) First Assignment should be submitted before the conduct of the first mid-term examinations, and the Second Assignment should be submitted before the conduct of the second mid-term examinations. The Assignments shall be as specified by the concerned subject teacher.

d) The first mid-term examination Marks and the second mid-term examination Marks shall make set of mid-term examination Marks; and the better of these two sets of marks shall be taken as the final marks secured by the Student towards mid-term examination. For Continuous Assessment, Assignment, Attendance and General Proficiency shall be considered in that Theory Subject.

e) For Practical Subjects, there shall be a Continuous Assessment based on Performance,, Attendance and General Proficiency and Lab./ Practical's Semester End Examination. The Semester End Examination for Lab./ Practical shall be conducted at the end of the Semester by the concerned Lab teacher of the same Department as assigned by the Head of the Department and External Examiner assigned by the University.

f) For Part Time Courses, there shall be a Seminar Presentation in III, IV and V Semesters, for the Seminar, the Student shall collect the information on a specialized topic, prepare a Power Point Presentation and submit to the Department at the time of Seminar Presentation. The Continuous Assessment given by the faculty handling the Seminar. The Presentation shall be evaluated by Committee Consisting Head of the Department and Senior faculty assigned by Head of the Department.

Dissertation :

Registration of Dissertation: The Project shall start immediately after the completion of II year IV semester in case of Part Time Course. Every Student must compulsory register for his M.Tech. Project Work, within the 4 weeks after the completion of II year IV semester in case of

Part Time Course. The student registered for the Project work shall work for two semesters. After Registration, the Student has to present in Dissertation-I in consultation with his Project Guide the title, objective and plan of action of his project work to the Project Review Committee (PRC-I) for approval within 6 weeks after the II year IV semester in case of Part Time Course. Only after obtaining the approval of the PRC, the student can initiate the Project work.

A Project Review Committee (PRC) shall be constituted by Head of the Department and shall consist of the Head of the department (Chairperson), Project Guide and one senior faculty member of the Department.

If a student wishes to change his Guide or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/Guide leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Guide or topic as the case maybe.

Dissertation-I: There shall be a Dissertation-I during the IV Semester (II Year) in case of Part Time Course. The Dissertation-I shall be evaluated by the PRC for Project guide will give Continuous Assessment marks and thereafter the Student shall appear in the Semester End Examination shall If he fails to obtain the minimum marks, he has to reappear for the Dissertation- I during the supplementary examinations.

Dissertation-II: There shall be a Dissertation-II & III during the V& VI Semester (III Year) in case of Part Time Course. The Dissertation-II shall be evaluated by the PRC to decide whether the Project is eligible for final submission or not and thereafter Project guide will give Continuous Assessment marks. After Final Submission, Dissertation will be sent for External Evaluation and approval. On External Approval, the Student shall appear in the Semester End Examination for success full completion. If he fails to obtain the minimum marks, he has to reappear for the Dissertation- I during the supplementary examinations as on when conducted.

Dissertation-I, II and II shall be conducted as per the schedule. The unsuccessful student may be given one more chance as Supplementary. Supplementary will be conducted only for unsuccessful students. The unsuccessful students in **Dissertation-I** shall reappear for it at the time of **Dissertation-II &III** as supplementary student. **These students shall reappear for Dissertation-III in the next academic year at the time of Dissertation-II only after successful completion of Dissertation-II.** The unsuccessful students in Project Work Review III shall reappear for Project Work Review III in the next academic year only at the time of Project Work Review II as supplementary students.

After successful completion of **Dissertation-III**, a soft copy of the project should be submitted to the Head of the Department for the ANTIPLAGIARISM check. The Head of the Department should carry out plagiarism check and submitted the report to the Principal. The Dissertation will be accepted for submission, if the similarity index is less than 20%. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re-submit the soft copy of the Dissertation after one month. The maximum number of re-submissions of Dissertation after plagiarism check is limited to TWO.

The Student shall be allowed to submit his Project Dissertation, only on the successful completion of all the prescribed PG Subjects (Theory and Practical's.), Seminar, etc. and after obtaining all approvals from PRC.

The Dissertation will be adjudicated by an external examiner selected by the University. For this the Head of the Department shall submit a panel of three examiners from among the list of experts in the relevant specialization as submitted with the help of project supervisor concerned. In such cases, the M.Tech. Dissertations will be sent to an External Examiner nominated by the Principal of the College, on whose 'approval', the Student can appear for the M.Tech. External Project Viva-voce Examination, which shall be conducted by a Board, consisting of the PG Project Supervisor, Head of the Department, and the External Examiner who adjudicated the M. Tech. Project Work and Dissertation. The Board shall jointly declare the Project Work Performance as 'satisfactory', or 'unsatisfactory'; and in successful cases, the External Examiner shall evaluate the Student's Project Work presentation and performance for stipulated Marks.

If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of External Project Viva-Voce examination. The External Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Dissertation. The student has to secure a minimum of 50% of marks in external Project (Viva-Voce) examination.

b) If he /she fail to fulfill the requirements as specified, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his project work by the board within a specified time period (within four years from the date of commencement of his first year first semester).

c) Ifthestudent'soralpresentationisnotsatisfactory,theboardmaydeferitandthe Student has to re-appear for the oral presentation before the same board for the award of degree.

d) The External Project Viva-Voce External examination marks must be submitted to the University on the day of the examination.

Re-Admission /Re-Registration:

Re-Admission for Discontinued Students:
Students, who have discontinued the M.Tech. Degree Programme due to any reasons what so ever, may be considered for 'Readmission' into the same Degree Programme (with same specialization) with the Academic Regulations of the Batch into which he gets Re-admitted, with prior permission from the concerned authorities.

Re-Registration for Detained Students:
When any Student is detained in a Subject (Theory / Practical / Seminar etc.) due to shortage of attendance in any Semester, he may be permitted to re-register for the same Subject in the 'same category' (Core or Elective Group) or equivalent Subject if the same Subject is not available, as suggested by the Board of Studies of that Department, as when offered in the sub-sequent Semester(s), with the Academic Regulations of the Batch into which he seeks re-registration , with prior permission from the concerned authorities, subject to Item.

Award of Degree and Class:
A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP),and secures the required number of 80 credits in case of Full Time Course

and 70 credits in case of Part Time Course, shall be declared to have 'QUALIFIED' for the award of the M.Tech.DegreeinthechosenBranchofEngineeringandTechnologywithspecialization as he wasadmitted.

Withholding of Results:

If a Student has not paid fees to University at any stage, or has pending dues against his name due to any reason whatsoever, or if any case of indiscipline is pending against him, the result of the Student may be withheld, and he will not be allowed to go into the next higher Semester. The Award or issue of the Degree may also be withheld in such cases.

Transitory Regulations:

A Student - who has discontinued for any reason, or who has been detained for want of attendance as specified, or who has failed after having undergone PGP, may be considered eligible for readmission to the same PGP with same set of Subjects/ Courses (or equivalent Subjects/ Courses as the case may be), and same Professional Electives (or from same set/category of Electives or equivalents as suggested), as and when they are offered (within the time-frame of 4 years from the Date of Commencement of his I Year I Semester).

Student Transfers:

There shall be no Branch/ Specialization transfers after the completion of Admission Process.

There shall be no transfer among the Constituent Colleges and Units of Rama Universti

Scope:

(i) Where the words "he, "him", "his", occur in the write-up of regulations, they include "she", "her", "hers".
(ii) Where the words "Subject" or "Subjects", occur in these regulations, they also imply "Course" or "Courses".
(iii) The Academic Regulations should be read as a whole, for the purpose of anyone predation.
(iv) In case of any doubt or ambiguity in the interpretation of the above regulations, the decision of the Vice-Chancellor / Dean is final.
(v) The College may change or amend the Academic Regulations, and/ or Course Structure, and/ or Syllabi at any time, and the changes or amendments made shall be applicable to all Students with effect from the dates as notified by the University.

17. **MALPRACTICESRULES**:

S.No.	Nature of Malpractices	Punishment
	If the student:	

1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the student which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
1 (b)	Gives assistance or guidance or receives it from any other student orally or by any other body language methods or communicates through cell Phones with any student or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the students involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or Practical) in which the student is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted to appear forth remaining examinations of the subjects of that Semester/year. The Hall Ticket of the student is to be cancelled.

S.No.	Nature of Malpractices	Punishment
	If the student:	
3	Impersonates any other student in Connection with the examination.	The student who has impersonated shall be expelled from examination hall. The student is also debarred and forfeits the seat. The performance of the original student who has been impersonated, shall be cancelled in all the subjectsof the examination(including Practical and Project Work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the student is subject to the academic regulations in Connection with forfeiture of seat.
7	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the student has appeared including practical examinations and project work of that semester / year examinations.
S.No.	**Nature of Malpractices**	**Punishment**
	If the student:	
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not

		be permitted for the remaining examinations of the subjects of that Semester/year. The student is also debarred and forfeits the seat.
9	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the student(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The students also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year.

S.No.	Nature of Malpractices	Punishment
	If the student:	
11	If student of the college, who is not a student for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects Of that semester/year. The student is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment	

18. GENERAL:

- Credit: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.
- The Academic Regulations should be read as a whole for the purpose of any interpretation.
- The University reserves the right of altering the Academic Regulations and/or Syllabus/Course Structure, as and when necessary. The modifications or amendments may be applicable to all the students on rolls, as specified by the University.
- Wherever the words 'he' o r 'him' or 'his' occur in the above regulations, they will also include 'she' or 'her' or' hers'.
- Wherever the word 'Subject' occurs in the above regulations, it implies the'Theory Subject', 'Practical Subject' or 'Lab.' and 'Seminar'.
- In case of any ambiguity or doubt in the interpretations of the above regulations, the decision of the Vice-Chancellor will be final.

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DK

COURSE STRUCTURE

M. TECH. (Part Time)

MICROELECTRONICS & VLSI DESIGN

Under

Choice Based Credit System (CBCS)

Program Educational Objectives (PEO's):

PEO1: To produce Microelectronics & VLSI Design post graduates, who are employable in public and private industries/ Institutes/Organization, or pursue higher education.

PEO 2: To prepare graduates who have the ability to identify and address current and future problems in the domain of electronic, microelectronics and VLSI design.

PEO 3: To inculcates research attitude and lifelong learning among graduates.

PEO 4: Students should be able to acquire knowledge for realizing it into gainful employment or entrepreneurship being useful to the societal needs.

Program specific outcomes (PSOs):

PSO 1 - Students will be proficient in designing, developing and analyzing the VLSI Design and their applications.

PSO2 - Students will be expertise in state-of-art simulation tools and real-time control platforms and exposure to multidisciplinary collaborative research works to emphasis their skills to attain key positions in research centers and industry or to emerge as entrepreneur.

PSO3 - Students will be able to assimilate in depth knowledge in power industry to obtain optimal solutions to complex problems.

PSO4 - Students are imbibed with ethical and social responsibilities in their professional endeavors.

Program Outcomes (PO's):

POs are defined for the program is aligned with the graduate attributes as follows:

PO 1: Acquire in-depth knowledge in the domain of Microelectronics & VLSI Design or professional area with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge.

PO 2: Ability to critically analyze various Microelectronics & VLSI Design components, models and their operation.

PO 3: Ability to apply fundamentals and concepts to analyze, formulate and solve complex problems of electrical Microelectronics & VLSI Design and its components.

PO4: Apply advanced concepts of VLSI Design to analyze, design and develop electronic3s components, apparatus and systems and to put forward scientific findings at national and international levels.

PO 5: Ability to use advanced techniques, skills and modern scientific and engineering tools for professional practice.

PO 6: Preparedness to lead a multidisciplinary scientific research team and communicate effectively.

PO 7: Demonstrate and apply knowledge and understanding of engineering principles for project management.

PO 8: To motivate exploring ideas and to encourage for independent, reflective and lifelong learning.

PO 9: The in-depth education necessary to understand the impact of engineering solutions in a global, economic, environmental and societal context.

PO 10: Ability to contribute to the community for sustainable development of society.

PO 11: Ability to learn from mistakes without depending on external feedback.

First Semester

S. NO.	Course Type	CODE	SUBJECT	TEACHING SCHEME			EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HRS/WK
				L	T	P	CA	MTE	ETE			
1.	Program Core	MECPC-101	Semiconductor Device Modeling	3	1	0	30	20	100	150	4	5
2.	Program Core	MECPC-102	Architectural Design of ICs	3	1	0	30	20	100	150	4	5
3.	Program Elective		Program Elective-1	3	1	0	30	20	100	150	4	5
PRACTICALS												
5.	Program Core	MECPC-151	Logic Design Lab	0	0	4	-	20	30	50	2	2
6.	Program Elective		Program Elective-1	0	0	4	-	20	30	50	2	2
			TOTAL	**9**	**3**	**8**	**90**	**100**	**360**	**550**	**16**	**19**

Second Semester

S. NO.	Course Type	CODE	SUBJECT	TEACHING SCHEME			EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HRS/WK
				L	T	P	CA	MTE	ETE			
1.	Program Core	MECPC-103	Digital VLSI Circuit	3	1	0	30	20	100	150	4	5
2.	Program Core	MECPC-104	Advance Microprocessor & Microcontroller	3	1	0	30	20	100	150	4	5
3.	Program Elective		Program Elective-2	3	1	0	30	20	100	150	4	5
PRACTICALS												
6.	Program Core	MECPC-152	Advance Microprocessor & Microcontroller Lab	0	0	4	-	20	30	50	2	2
7.	Program Elective		Program Elective-2	0	0	4	-	20	30	50	2	2
			TOTAL	**9**	**3**	**8**	**90**	**100**	**360**	**550**	**16**	**19**

Third Semester

S. NO.	Course Type	CODE	SUBJECT	TEACHING SCHEME			EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HRS/WK
				L	T	P	CA	MTE	ETE			
1.	Program Elective		Program Elective-3	3	1	0	30	20	100	150	4	5
2.	Open Elective		Open Elective-1	3	1	0	30	20	100	150	4	5
PRACTICALS												
3.	Program Elective		Program Elective-3	0	0	4	-	20	30	50	2	2
			TOTAL	**6**	**2**	**0**	**60**	**60**	**230**	**350**	**10**	**12**

Fourth Semester

S. NO	Course Type	CODE	SUBJECT	TEACHING SCHEME			EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HRS/WK
				L	T	P	CA	MTE	ETE			
1.	Program Elective		Program Elective-4	3	1	0	30	20	100	150	4	5
PRACTICALS												
3.	Dissertation	MECPD 101	Dissertation I	0	0	8	-	100	200	300	7	10
			TOTAL	**3**	**1**	**8**	**30**	**120**	**300**	**350**	**11**	**13**

Fifth Semester

S. NO.	Course Type	CODE	SUBJECT	TEACHING SCHEME			EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HRS/WK
				L	T	P	CA	MTE	ETE			
1.	Open Elective		Open Elective-1	3	1	0	30	20	100	150	4	5
PRACTICALS												
3.	Dissertation	MECPD 102	Dissertation II	0	0	8	-	100	200	300	7	10
			TOTAL	**3**	**1**	**8**	**30**	**120**	**300**	**450**	**11**	**13**

Six Semesters

S. NO.		CODE	SUBJECT	TEACHING SCHEME			EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HRS/WK
				L	T	P	CA	MTE	ETE			
PRACTICALS												
3.	Project	MECPD 103	Dissertation III	0	0	24	-	200	300	500	16	12
			TOTAL	**0**	**0**	**24**	**00**	**200**	**300**	**500**	**16**	**12**

Program Core

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE-REQUISITES
			L	T	P	J	CA	MTE	ETE				
THEORY													
1.	MECPC 101	Semiconductor Device Modeling	3	1	0	0	30	20	100	150	4	5	
2.	MECPC 102	Architectural Design of ICs	3	1	0	0	30	20	100	150	4	5	
3.	MECPC 103	Digital VLSI Circuit	3	1	0	0	30	20	100	150	4	5	
4.	MECPC 104	Advance Microprocessor & Microcontroller	3	1	0	0	30	20	100	150	4	5	
PRACTICALS													
8.	MECPC -151	Logic Design Lab	0	0	4	0	-	20	30	50	2	2	
9.	MECPC -152	Advance Microprocessor & Microcontroller Lab	0	0	4	0	-	20	30	50	2	2	

Program Elective

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE-REQUISITES
			L	T	P	J	CA	MTE	ETE				
Bouquet: Elective I													
THEORY													
1.	MECPE101	Analog VLSI Design	3	1	0	0	30	20	100	150	4	5	
2.	MECPE102	Advanced Data Communication Network	3	1	0	0	30	20	100	150	4	5	
3.	MECPE103	Switching Theory and Logic Design	3	1	0	0	30	20	100	150	4	5	
4.	MECPE104	CAD of VLSI Design	3	1	0	0	30	20	100	150	4	5	
PRACTICALS													
5	MECPE -151	VLSI Design Lab	0	0	4	0	-	20	30	50	2	2	

Program Elective

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE-REQUISITES
			L	T	P	J	CA	MTE	ETE				
Bouquet: Elective III													
THEORY													
1.	MECPE201	VLSI Technology	3	1	0	0	30	20	100	150	4	5	
2.	MECPE202	Advanced Signal Processing	3	1	0	0	30	20	100	150	4	5	
3.	MECPE203	Artificial Neural Network	3	1	0	0	30	20	100	150	4	5	
4.	MECPE204	Nano Technology	3	1	0	0	30	20	100	150	4	5	
PRACTICALS													
5.	MECPE -251	Analog IC Design Lab	0	0	4	0	-	20	30	50	2	2	

Program Elective

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE-REQUISITES
			L	T	P	J	CA	MTE	ETE				
Bouquet: Elective II													
THEORY													
1.	MECPE301	Low Power VLSI Design	3	1	0	0	30	20	100	150	4	5	
2.	MECPE302	Memory Technologies	3	1	0	0	30	20	100	150	4	5	
3.	MECPE303	Artificial Intelligence	3	1	0	0	30	20	100	150	4	5	
4.	MECPE304	Micro-controller based system design	3	1	0	0	30	20	100	150	4	5	
PRACTICALS													
5.	MECPE -351	VLSI CAD Lab	0	0	4	0	-	20	30	50	2	2	

Program Elective

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE-REQUISITES
			L	T	P	J	CA	MTE	ETE				
Bouquet: Elective IV													
THEORY													
1.	MECPE401	Fault Tolerant Digital Design	3	1	0	0	30	20	100	150	4	5	
2.	MECPE402	Advance Computer Architecture	3	1	0	0	30	20	100	150	4	5	
3.	MECPE403	Pattern Recognition	3	1	0	0	30	20	100	150	4	5	

Dissertation

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE-REQUISITES
			L	T	P	J	CA	MTE	ETE				
PRACTICALS													
1.	MECPD 101	Dissertation I	0	0	8	0	-	100	200	300	7	10	
2.	MECPD 102	Dissertation II	0	0	8	0	-	100	200	300	7	10	
2.	MECPD 103	Dissertation III	0	0	24	0	-	200	600	800	16	12	
TOTAL			**0**	**0**	**40**	**0**	**-**	**400**	**1000**	**1400**	**30**	**0**	

Open Elective -1

S. NO.	CODE	SUBJECT	TEACHING SCHEME				EVALUATION SCHEME			TOTAL MARKS	CREDITS	CONTACTS HR/WK	PRE REQUISITES
			L	T	P	J	CA	MTE	ETE				
THEORY													
1.	MEC0E101	Design of Digital IC	3	1	0	0	30	20	100	150	4	5	
2.	MEC0E102	Micro Electro Mechanical System	3	1	0	0	30	20	100	150	4	5	
3.	MEC0E103	Information Security	3	1	0	0	30	20	100	150	4	5	
4.	MEC0E104	Compound Semiconductors	3	1	0	0	30	20	100	150	4	5	

MECPC 101: SEMICONDUCTOR DEVICE MODELING

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. To understand operation of semiconductor devices.
2. To verify the BJT modeling & simulation techniques.

Unit	Topic	No. of Lecture
Unit I	Electrons and holes in silicon, p-n junction, MOS capacitor, High field effects. MOSFET Devices, Long-channel MOSFETs, Short-channel MOSFETs. CMOS Device Design: MOSFET Scaling, Threshold voltage, MOSFET channel length. Static model, Large signal model and SPICE models,	**8**
Unit II	BJT modeling: Ebers Moll, Static, large-signal, small- signal models. Gummel - Poon model. Temperature and area effects. Power BJT model, SPICE models, Limitations of GP model; Advanced Bipolar models: VBIC, HICUM and MEXTARM; MOS Transistors: LEVEL 1, LEVEL 2 ,LEVEL 3, BSIM, HISIMVEKV Models	**8**
Unit III	Threshold voltage modeling. Punch through. Carrier velocity modeling. Short channel effects. Channel length modulation. Barrier lowering, Hot carrier effects.	**8**
Unit IV	Mobility modeling, Model parameters; Analytical and Numerical modeling of BJT and MOS transistors:	**8**
Unit V	Introduction to various simulation techniques, Noise modeling; Modeling of hetero-structure devices.	**8**

Course Learning Outcomes (CLO):

1. Clear understanding & utilization of MOS & semiconductor microwave devices.
2. Design and develop different advanced electronic devices.

Text Book:

1. Ben G Streetmen and Sanjay Kumar Benerjee, "Solid State Electronics Device" PHI publication.
2. Muller and Kamins, "Device Electronics for Integrated Circuits", John Welley and sons.

Reference Books:

1. Millman J. and Halkias .C., " Integrated Electronics ", Tata McGraw-Hill.
2. Robert L. Boylestad and Louis Nashelsky, 8th edn. PHI.
3. S. Salivahanan, et.al, "Electronic Devices and Circuits", TMH.
4. Floyd, Electronic Devices, Sixth edition, Pearson Education.
5. I.J. Nagrath, Electronics - Analog and Digital, PHI.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2		1			2	2		2
2	2	1	3	2						2	1

MECPC 102: ARCHITECTURAL DESIGN OF ICS

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet with the objectives of

1. To teach fundamentals of VLSI circuit design and implementation using circuit simulators and layout editors.
2. To implement combinational and sequential circuits using VHDL

Unit	Topic	No. of Lecture
Unit I	Introduction: VLSI Design flow, Review of VLSI Design flow. Goals of VLSI Design: Optimization of speed, power dissipation, cost and reliability, general design methodologies; Mapping algorithms into Architectures: Signal flow graph, data dependences, data path synthesis, control structures, critical path and worst case timing analysis.	**10**
Unit II	Hardware Description Languages: Basic concepts of hardware description languages, Hierarchy, modeling, Structural, Data-flow and Behavioral styles of hardware description, Syntax and Semantics of VHDL, Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Modules, nets and registers, • Concurrent and sequential constructs, Examples of design using VHDL & Verilog.	**8**
Unit III	Pipeline and parallel architectures: Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures	**9**
Unit IV	Control strategies: Hardware implementation of various control structures, VLIW architecture; Testable architecture: Controllability and observability, boundary scan and other such techniques, identifying fault locations, self reconfigurable fault tolerant structures.	**6**
Unit V	Data path elements: Data path design philosophies, fast adder, multiplier, driver etc., data path optimization, application specific combinatorial and sequential circuit design, CORDIC unit.	**7**

Course Learning Outcomes (CLO):

Upon Completion of the topics:

1. Realize logic circuits with different design styles.
2. Simulate and implement combinational and sequential circuits using VHDL systems.
3. Model digital systems in VHDL and System C at different levels of abstraction.

Text Book:

1. C.Y. Chang and S.M. Sze (Ed), ULSI Technology, McGraw Hill.
2. *Digital circuits* and *logic design, Samuel C. Lee*, PHI.
3. William I. Fletcher," An Engineering Approach to Digital Design", Prentice Hall India.
4. Hill & Peterson, "Switching Circuit & Logic Design", Wiley.
5. Charles H Roth Jr, "Digital System Design using VHDL", Thomson Learning, 2002.
6. Douglas L Perry, "VHDL: Programming by Example", TMH publication.
7. Jayram Bhaskar, "VHDL Primer", TMH Pub.
8. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing, Allentown, PA) 1998.

Reference books:

1. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall (NJ, USA), 1996.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2		1			2	2		2
2	2	1	3	2						2	1
3	3	2	1	1						1	

MECPE 101: ANALOG VLSI DESIGN

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet with the objectives of

1. To teach fundamentals of analog VLSI design and implementation.
2. To study the feedback amplifier & high frequency amplifier.

Unit	Topic	No. of Lecture
Unit I	**SINGLE STAGE AMPLIFIERS:** Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower cascocde and folded cascade configurations, differential amplifiers and current mirror configurations.	**8**
Unit II	**HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS:** Current mirrors, cascode stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers	**8**
Unit III	**FEEDBACK AND OPERATIONAL AMPLIFIERS:** Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.	**8**
Unit IV	**STABILITY AND FREQUENCY COMPENSATION:** General considerations, Multipolesystems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.	**8**
Unit V	**BANDGAP REFERENCES:** supply independent biasing, temperature independent references, PTAT currentgeneration, Constant-Gm Biasing.	**8**

Course Learning Outcomes (CLO):

Upon Completion of the topics:

1. Realize logic circuits with different design.
2. Understand MOS basic feedback, high frequency of differential amplifier.
3. Able to explain bandgap references.

Text Book:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill
2. Willey M.C. Sansen, "Analog Design Essentials", Springer.

Reference books:

3. Gray and Mayer "Analysis and Design of Analog Integrated circuit", Welly India.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons, Inc.
5. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second edition, Oxford.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	2	2	3		1			2	2		2
2	2		2	2						2	
3	3	2	1	1						1	

MECPE 201: VLSI TECHNOLOGY

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. This course introduces the theory and technology of micro/nano fabrication. Because of the interdisciplinary nature of the subject, its content includes concepts from many disciplines in engineering (electrical, materials, mechanical, chemical) and science. In lecture, we will discuss the theory of basic processing techniques, such as diffusion, oxidation, photolithography, chemical vapor deposition, physical vapor deposition, etching, and metallization.
2. In the labs section of this course, we will be fabricating three different devices; an MOS capacitor, a micro cantilever, and a micro fluidic device. You will test each device in the lab and prepare a laboratory report for each device.
3. At the end of this course, one should have a good understanding of the various processing techniques used to micro/nano fabricate. One should understand the theory of the individual processes, how they are characterized, and the interrelationship of these processes when combined to fabricate devices.

Unit	Topic	No. of Lecture
Unit I	Semiconductor review and survey of IC processing Roadmap; Concepts of Clean room and safety requirements, Concepts of Wafer cleaning processes and wet chemical etching techniques. Silicon crystal growth and wafer preparation.	**9**
Unit2	Unit Processes : Substrate cleaning , Oxidation ; Doping techniques: Diffusion, Ion implementation ;	**7**
Unit 3	Pattern transfer: mask making & different lithography techniques (optical, x-ray, E-Beam, Ion-Beam); Vacuum science & plasmas; Etching: Isotropy, anisotropy, selectivity, wet plasma, RIBE etc.;	**8**
Unit 4	Thin films: Physical deposition, evaporation and sputtering; Chemical Vapor Deposition: CVD, LPCVD, PECVD, MOCVD, MBE etc. ; Epitaxial growth; Lithography: optical, electron beam, X-ray etc.	**8**

Unit 5	Process integration: Device isolation technology (junction, dielectric, LOCOS, trench etc); Advances in Bipolar, MOS and BICMOS process technologies; A case study using process simulation tools.	8

Course Learning Outcomes (CLO):

At the end of this module, students are expected to be able to:

1. To develop knowledge and an understanding of micro and nano fabrication technologies, processes and their applications
2. Demonstrate understanding of specific nanofabrication approaches

Text Books:

1. C.Y. Chang and S.M. Sze (Ed), ULSI Technology, McGraw Hill.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	2	2	3		1			2	2		2
2	2		2	2						2	

MECPE 151: VLSI DESIGN LAB

L	T	P	CR
0	0	4	2

Analog Design Flow

1. Design an Inverter with given specifications*, completing the design flow
   Mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design. Verify & Optimize for Time, Power and Area to the given constraint
2. Design the following circuits with given specifications*, completing the
   Design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

   i) AND, OR, NOR, NAND, XOR, XNOR with using of MOS technology.

3 Design the following circuits with given specifications*, completing the
   Design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

i) Combinational circuit with using of MOS technology.

4 Simulate a static CMOS circuit to compute f = (A+B) (C+D) with least each input can present a maximum of 30 lambda of transistor width. The output must drive a load equivalent to 500 lambda of transistor width. Choose transistor size to achieve least delay and estimate the delay in t.

Course Learning Outcomes (CLO):

At the end of this module, students are expected to be able to:

1. Design, verify & understanding of different type of logic gates & combinational circuits.
2. Understand the significance of different biasing styles and apply them apply for different circuits.
3. Simulate a static CMOS circuit & analysis the circuit to achieve least delay.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1					3	2	2		1	2	2
2					3	1	2			2	2
3					3	3	1		2		

MECPC 151: LOGIC DESIGN LAB

L	T	P	CR
0	0	4	2

1. HDL code to realize all the logic gates.
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design and analysis of 4 bit binary to gray converter.
4. Design and analysis of Multiplexer/ Demultiplexer, comparator.
5. Design and analysis of Full adder using 3 modeling styles.
6. Design and analysis of flip flops: SR, D, JK, T.
7. Design and analysis of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter.
8. Design and analysis of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
9. Design and analysis of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
10. Design and analysis of 4- Bit Multiplier, Divider.
11. Design and analysis of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication and Division.
12. Design and analysis of Finite State Machine.
13. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Course Learning Outcomes (CLO):

At the end of this module, students are expected to be able to:

1. Design & analysis of different type of combinational & sequential circuits.
2. Synthesize digital circuit using HDL code.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1					3	2	2		1	2	2
2					3	1	2			2	2

MECPC 103: DIGITAL VLSI CIRCUIT

L	T	P	CR
3	1	0	4

Course Objectives:

1. To understand how a digital IC is designed under VLSI technology
2. Application of SRAM, DRAM & RRAM in industry

Unit	Topic	No. of Lecture
Unit I	Issues of Digital IC Design: General overview of design hierarchy, layers of abstraction, integration density and Moore's law, VLSI design styles, VLSI hierarchy, Regularity, Modularity and Locality, VLSI Design Flow.	7
Unit II	Logic Design: switch logic, gate restoring logic, Programmable Logic Array (PLAs), Finite State Machine (FSM) as a PLA, personality matrix of a PLA, PLA folding, pseudo-nmos logic, BiCMOS logic gates; Basic Circuit Concepts: sheet resistance and area capacitances of layers, driving large capacitive loads, super-buffers, propagation delay models of cascaded pass transistors, wiring capacitances, switching delay in BiCMOS logic circuits; Bipolar ECL.	8
Unit III	Inverter : features of ECL gate, robustness and noise immunity, logic design in ECL, single-ended and differential ECL gates; Dynamic CMOS design : steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, np-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme, different logic families like CPL, DCVSL etc.	**9**
Unit IV	Sequential CMOS Logic Circuits: basic regenerative circuits, digital phase-locked loop (DPLL); Low-power CMOS Logic Circuits: low-power design through voltage scaling, estimation and optimization of switching activity, reduction of switched capacitance, adiabatic logic circuits; Subsystem Design: design of arithmetic building blocks like adders and multipliers, barrel and logarithmic shifters, area-time tradeoff, power consumption issues.	**9**
Unit V	Semiconductor Memories : Dynamic Random Access Memories (DRAM), Static RAM, non-volatile memories, flash memories, low-power memory; Case Study *(instructor may choose any suitable digital system; in the following, an example is suggested)* : A RISC Processor - Instruction Set, Pipeline Architecture, Major Logic Blocks, Layout, Functional Verification.	**7**

Course Learning Outcomes (CLO):

After finishing of this course the students will be able to -

1. Solve problems occurs in different VLSI industry.
2. Solve application specific digital IC testing
3. Discuss the high density memory packaging.
4. Students will be substantially prepared to take up prospective research assignments.

Text Book:

1- *Digital* Integrated *Circuits*. Sung-Mo *Kang*, Yusuf Leblebici. Tata McGraw-Hill
2- - *Digital* Integrated *Circuits VLSI-Rabaey* - *Digital* Integrated *Circuits*.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2						2		2
2	3	3	2				2				
3	2	3	1	2							2
4	3	2	2								

MECPC 104: ADVANCE MICROPROCESSOR & MICROCONTROLLER

L	T	P	CR
3	1	0	4

Course Objectives:

The course is design to meet with the objectives of:

1. To study the Architecture of microprocessor 8086
2. To study the programming of 8086 using C.
3. To study the architecture of INTEL 8051.

Unit	Topic	No. of Lecture
Unit I	8085 Microprocessor architecture – signals – Addressing modes – Instruction classification Instruction set—Timing diagram – ALP format – Programming 8085 – 8-bit and 16-bit Operation including stack-subroutine. **Introduction to 8086 microprocessor:** Architecture of 8086 (Pin diagram, Functional block diagram, Register organization Arithmetic operations, Logic Operations, Branch operation.	7
Unit II	Program structure of 8086, 8086 instruction, Assembler Directives, string, procedures & macros, 8086 interrupts and interrupt applications, Interfacing.	9
Unit III	Microcomputer system peripherals, Introduction of 80386 microprocessors, scheduling, memory management, mode of operation, call gate, privilege levels, Interrupt and Exception handling, Paging, introduction to Pentium Processors.	7
Unit IV	INTEL 8051 architecture, instruction set and programming, Memory mapping, addressing modes, Registers, expanded modes. Interrupt handling timing and serial I/O. Design and application of Micro-Controller in Data acquisition, Embedded controllers, Process control etc.	9
Unit V	**Programming techniques in C:** looping, counting and indexing, Programmable peripheral interface, interfacing keyboard and seven segment display and other output devices, 8051 serial port programming.	8

Course Learning Outcomes (CLO):

1. Understanding basic principle of microprocessor.
2. Microprocessor programming and interfacing.
3. Understand efficiency in microprocessor-based system.
4. Write code or a compiler for a microprocessor which takes advantage of the advanced architectural techniques.

Text and Reference Books:

1. Douglas V Hall "Microprocessors and interfacing" TMH Publication.
2. Muhammad Ali Mazidi "The 8051Microcontroller and Embedded System" TMH Publication.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2						2	1	
2	2		2				2				
3	2	3	1	2						2	2
4		2	2						1		2

MECPE 301: LOW POWER VLSI DESIGN

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet with the objectives of

1. To understand the basics of MOS in different regions of operation and to understand how to apply proper bias voltages so as to operate as a switch or amplifier.
2. To understand the operations of CAD tools in the design and analysis of low power CMOS circuits.

Unit	Topic	No. of Lecture
Unit I	**Introduction to VLSI design:** MOS Physics, Structure and operation of MOSFETs, MOSFET current- voltage characteristics, MOSFET Modeling, MOSFET Scaling, MOSFET Capacitances.	9
Unit II	**Low Power Design:** Introduction, Needs of Low power VLSI chips, dynamic power dissipation, short circuit power dissipation, leakage power dissipation. Review of power dissipation in CMOS Circuits – static and dynamic power dissipation Leakage sources.	8
Unit III	**MOSFET Scaling: constant** field scaling, constant voltage scaling, limitations on scaling of MOSFET, comparison between constant field and constant voltage scaling, advantages of scaling, disadvantages of scaling.	7
Unit IV	**Low–Power CMOS Logic Circuits:** Introduction, Low – Power Design through voltage scaling, Variable threshold CMOS Circuits, Multiple threshold CMOS circuits, Estimation and Optimization of switching activity, Reduction of Switched Capacitance and Adiabatic Logic Circuits. **POWER ESTIMATION:** Power Estimation techniques, logic power estimation, Simulation power analysis, Probabilistic power analysis.	**9**
Unit V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER:** Synthesis for low power – Behavioral level transform – software design for low power.	7

Course Learning Outcomes (CLO):

Upon Completion of the topics:

1. Students will be able to bias MOS transistors depending on requirements.
2. Knowledge about operations of low power CMOS circuits.

Text Books:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer.

Reference Books:

3. J.B. Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley.
4. A.P .Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design" Kluwer.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2	1							2
2	3	3	1	3						2	2

MECPE 351: VLSI CAD LAB

L	T	P	CR
0	0	4	2

1- Design the following circuits with given specifications*, completing the Design flow mentioned below:

a. Draw the schematic and verify the following
i) DC Analysis
ii) AC Analysis
iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design

i) AND, OR, NOR, NAND, NOT
ii) XOR, XNOR

2 Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following
   i) DC Analysis
   ii) AC Analysis
   iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

3 Design an comparator with given specification* using given differential amplifier Common Source and Common Drain amplifier in library** and completing the design Flow mentioned below:

a. Draw the schematic and verify the following
   i) DC Analysis
   ii) AC Analysis
   iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

4 Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library**.

a. Draw the schematic and verify the following
   i) DC Analysis
   ii) AC Analysis
   iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

5 For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verifies the functionality by completing ASIC Design

FLOW.

Course Learning Outcomes (CLO):

At the end of this module, students are expected to be able to:

1. Comprehend the stability issues of the systems and should be able to design OpAmp fully, Compensated against process, supply and temperature variations.
2. Design & analysis of comparator, DAC & verify their functionality.
3. Draw the layout of DRC, ERC & their verification.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1		3	2	2			2		3	2	
2		2	2				2		1	2	
3		2	1	2			1		2	2	

MECPE 251: ANALOG IC DESIGN LAB

L	T	P	CR
0	0	4	2

List of Experiments.

1. Common Source Amplifier
2. Cascade Amplifier
3. Push Pull Amplifier
4. Folded Cascade Amplifier .
5. Current Mirror.
6. Cascaded Current Mirror.
7. Differential Amplifier
8. CMOS Op-amp single Stage.
9. Common Drain Amplifier.
10. Common Gate Amplifier.
11. Current Controlled Voltage source.

Course Learning Outcomes (CLO):

At the end of this module, students are expected to be able to:

1. Comprehend the stability issues of the systems and should be able to design OpAmp fully. Compensated against process, supply and temperature variations.
2. Design & analysis of comparator, DAC & verify their functionality.
3. Draw the layout of DRC, ERC & their verification.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1		3	2	2			2		3	2	
2		2	2				2		1	2	
3		2	1	2			1		2	2	

MECPC 152: ADVANCED MICROPROCESSOR & MICROCONTROLLER LAB

L	T	P	CR
0	0	4	2

Experiments Based on Microprocessor (8086/8088)

Assembling and Executing the Program

1. Programs on Data Transfer Instructions.
2. Programs on Arithmetic and Logical Instructions.
3. Programs on Branch Instructions.
4. Programs on Subroutines.
5. Sorting of an Array.
6. Programs on Interrupts (Software and Hardware).
7. 8086 Programs using DOS and BIOS Interrupts.

Experiments Based on Interfacing & Microcontroller (8051)

8. DAC Interface of Waveform generations.
9. Stepper Motor Control.
10. Keyboard Interface / LCD Interface.
11. Data Transfer between two PCs using RS.232 C Serial Port.
12. Programs on Data Transfer Instructions using 8051 Microcontroller.

13. Programs on Arithmetic and Logical Instructions using 8051 Microcontroller.
14. Applications with Microcontroller 8051.

Course Learning Outcomes (CLO):

At the end of this module, students are expected to be able to:

1. To write a program & debugging related to 8086/8088 microprocessor.
2. How to control different function of stepper motor.
3. Transfer data between two PCs using different techniques.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1			2	2					2	2	1
2		2	2						1	2	2
3		2	1	2					2	2	2

MECPE 102: ADVANCED DATA COMMUNICATION NETWORK

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet with the objectives of:

1. To know Communication between applications on different computers,
2. To understand state-of-the-art in network protocols, architectures, and applications,
3. Examine and comprehend the following networking concepts -basic computer networking concepts including Circuit-switching and Packet-switching, Residential access networks (point-to-point, dialup modem, ADSL, cable modem), Protocol layer stack, Client-Server paradigm, and Packet-switched network delay calculation application-layer applications including Telnet, FTP, DNS, HTTP, SMTP - Other state of arts topics including Wireless and Mobile Networks, and Security in Computer Network.
4. Examine and analyze the following transport-layer concepts: -Transport-Layer services Reliable vs. un-reliable data transfer -TCP protocol - UDP protocol
5. Examine and synthesize the following network-layer concepts: -Network-Layer services –Routing -IP protocol -IP addressing
6. Examine and evaluate the following link-layer and local area network concepts: -Link-Layer services –Ethernet -Token Ring -Error detection and correction -ARP protocol.

Unit	Topic	No. of Lecture
Unit I	**Introduction to Data Communication and Networks**: Data Communication, Networks, Physical structures, different topologies, Categories of Networks: LAN, MAN, WAN, Interconnection of networks, The Internet. Protocols and Standards, Standards Organizations. Network Models, Layered tasks, The OSI model, different layers in OSI model. TCP/IP protocol suite ; Line Coding Scheme	7
Unit II	**Physical Layer:** Multiplexing, Frequency Division, Wavelength Division, Circuit Switched Networks, Datagram Networks, Virtual Circuit Networks, Structure of a switch, Ethernet Physical Layer,, HDLC, Point to Point Protocol.	**8**
Unit III	**Data Link Layer**: Introduction Types of Errors, Redundancy, Detection Vs Correction, Forward Error Correction Vs Retransmission, Block Coding Error Detection, Error Correction, Hamming Distance, Minimum Hamming Distance .Linear Block Codes, Cyclic Codes Cyclic Redundancy Check, Cyclic Code Analysis, Advantages. Checksum, Framing Fixed and Variable Size Flow and Error Control, Protocols, Noiseless Channels, Simplest and Stop and Wait Protocols. Noisy Channels, Stop and Wait Automatic Repeat Request, Go Back N Automatic Repeat Request, Selective Repeat Automatic Repeat Request. HDLC, Point to Point Protocol.	**7**
Unit IV	**Medium Access**: Random Access ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). Controlled Access Reservation, Polling, Token Passing. Channelization Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA). IEEE Standards, Standard Ethernet, Changes in the Standard, Fast Ethernet, Gigabit Ethernet, IEEE 802.11Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer. Bluetooth Architecture, Radio Layer, Baseband Layer, L2CAP.	**10**
Unit V	**Connecting LANs**: Connecting Devices Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Three Layer Switches, Gateway. Network layer logical addressing. IPv4AddressesAddress Space, Notation, Classful Addressing, Classless Addressing, IPv6 Addresses Structure and Address Space. Internetworking Need For Network Layer, IPv4Datagram,Fragmentation, Routing Delivery forwarding techniques and processes, routing table, Unicast routing, Multicast routing, Transport Layer Protocol : UDP and TCP, ATM, Cryptography, Network Security	**8**

Course Learning Outcomes (CLO):

1. Explain the roles of key elements in data communication.
2. Explain the difference between local area and wide area networks.
3. Explain the uses of WANs with respect of current practice.
4. Design Explain the uses, hardware requirements and advantages of WANs.
5. Describe the application and operation of protocols.
6. Distinguish types of networks.

Text Books:

1. B. A. Forouzan, "Data Communications and Networking", MGH, 4th ed.

Reference Books:

2. A. S. Tanenbaum, "Computer Networks", PHI.
3. W. Stallings, "Data and Computer Communication", PHI.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3								3	3	
2	3							2	3	2	
3	3								3	3	
4	3		1				2		3	2	2
5	2	2	1						2	2	
6	3	2	1							2	

MECPE 103: SWITCHING THEORY AND LOGIC DESIGN

L	T	P	CR
3	1	0	4

Course Objectives:

1. To study the sequential logic circuits design both in synchronous and Asynchronous modes for various complex logic and switching devices, their minimization techniques and their realizations.
2. To study the combinational logic design of various logic and switching devices and their realization.

Unit	Topic	No. of Lecture
Unit I	Vector switching algebra and Vector switching functions. Special class of switching functions: Threshold, Symmetric functions. Functions with decomposable properties, majority and monotonic functions. Logical completeness of switching functions and complete set of logic primitives.	**9**
Unit2	Hazards in combinational circuits and hazard free realization. Boolean differential calculus: Computation of Boolean derivatives and differentials.	**7**
Unit 3	**SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN:** Analysis of clocked synchronous sequential circuits, Moore/Mealy State diagrams, State Table, State Reduction and Assignment, Design of synchronous sequential circuits. **ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN:** Analysis of asynchronous sequential circuit, Cycles Races, Static, Dynamic and Essential hazards, Primitive Flow Table, State Reductions and State Assignment, Design of asynchronous sequential circuits.	**8**
Unit 4	Fault detection and location in combinational circuits: Tabular, ENF, Path Sensitizing and Boolean Difference methods.	**8**
Unit 5	Sequential machines: Initial uncertainty, successor tree and terminal nodes. Homing, distinguishing and synchronizing sequences Identifications of Sequential machines, checking experiments, Special classes of Sequential machines, Information lossless machine, definitely diagnosable machine and linear sequential circuits.	**8**

Course Learning Outcomes (CLO):

At the end of this module, students are able to

1. Design synchronous & asynchronous circuit.
2. Faculty detection in combinational circuit.

Text Books:

1. Switching and Finite Automata Theory by Zvi Kohavi and Niraj K. Jha, Tata Mc Graw Hill.
2. *Digital circuits and logic design, Samuel C. Lee*, PHI.
3. William I. Fletcher," An Engineering Approach to Digital Design", Prentice Hall India.
4. Hill & Peterson, "Switching Circuit & Logic Design", Wiley.

Reference Books:

5. Charles H. Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004.
6. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3							3	3	3	
2	3				1			2	3	2	2

MECPE 202: ADVANCED SIGNAL PROCESSING

L	T	P	CR
3	1	0	4

Course Objectives:

1. To make the students to understand different types of digital signal processing techniques and tools
2. To make students familiarization about advanced transform, namely discrete Z transform, Fast Fourier transform and Filters using MATLAB
3. To make students to apply transform and DSP techniques to design systems of coding & decoding

Unit	Topic	No. of Lecture
Unit I	Review of Discrete time signals: sequences, representation. Discrete time systems: linear, time in variant, LTI systems, properties, and constant coefficients difference equations. Frequency Domain representation of discrete time signals and systems.	7
Unit II	**Review of Z Transform** –Properties, ROC, Stability, Causality, Criterion. Inverse Z Transform, Recursive and Non Recursive systems, Realization of discrete time system.	8
Unit III	**Discrete Fourier Transforms:** Definitions, Properties of the DFT, Circular Convolution, Linear Convolution Discrete Cosine Transform, Relationship between DFT and DCT. Computation of DFT: FFT/Decimation in Time and Decimation in Frequency.	7
Unit IV	**Finite Impulse Response Filter Design:** Windowing and the Rectangular Window, Other Commonly Used Windows, Examples of Filter Designs Using Windows, The Kaiser Window Application of MATLAB for Design of Digital filter. Effect of Finite register length in filter Design.	8
Unit V	**Discrete time Random signals:** Discrete time random process, Averages, Spectrum Representation of finite energy signals, response of linear systems to random signals. Power spectrum estimation: Basic principles of spectrum estimation, estimate of auto con variance, power spectrum, cross con variance and cross spectrum. **Advance signal processing technique and transforms:** multi rate signal processing down sampling/up sampling, introduction to discrete Hilberts Transform, Wavelet Transform, Haar Transform etc.	10

Course Learning Outcomes (CLO):

At the end of this module, students are able to

1. Utilize the DSP tools and Techniques, Discrete Z transform, Fast Fourier Transform to design system & analysis
2. To design important filters FIR, IIR for systems and analysis.

Text /Reference Books:

1. Discrete time signal processing by Openheim & Schaffer PHI 2nd Edition.
2. Digital Signal Processing using MATLAB by S. Mitra.
3. Digital Signal Processing By Proakis Pearson Education.
4. Theory & application of Digital Signal Processing by L. R. Rabiner& B. Gold

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2							3	3	
2	3	2			1				3	2	2

MECPE 401: FAULT TOLERANT DIGITAL DESIGN

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. Acquire knowledge about fault tolerance in arithmetic circuits.
2. Learn about Fault diagnosis, Fault tolerance measurement.
3. Acquire knowledge on Software reliability models, and methods.

Unit	Topic	No. of Lecture
Unit I	**Basic Concept of Reliability:** Definition, Failure Rate, Relation between Mean time and Reliability, Maintainability, Availability, Series and Parallel System. **Faults in Digital Circuits:** Failures and Faults, Modeling of Faults- (Stuck at Faults, Bridging Faults, Stuck Open Faults), Temporary Faults.	8
Unit2	**Test Generation:** Fault Diagnosis of Digital Systems, Test Generation for Combinational Logic Circuits (One Dimension Path Sensitization, Boolean Difference, D- Algorithm, PODEM), Detection of Multiple Faults in Combinational Logic Circuits, Test Generation for Sequential Logic Circuits, Random Testing, Transition Count Testing, Signature Analysis.	8
Unit 3	**Fault Tolerant Design of Digital System:** Concept of Fault Tolerance, Static Redundancy, Dynamic Redundancy, Hybrid Redundancy, Self Purging Redundancy, Shift out Modular Redundancy, 5MR Reconfiguration Scheme, Fault Tolerant Design of Memory Systems using Error correcting codes, Time Redundancy, Software Redundancy, Fail Soft Operation, Fault Tolerant chip for Design of VLSI Chips.	8
Unit 4	**Self Checking and Fail Safe Logic:** Design of Totally Self Checking Checkers (Two Rail Checkers, Self Checking checkers for m-out –of – n Codes, Self Checking for Burger codes, Low cost residual code), Self Checking sequential Machine, Partially Self Checking Circuits, Fail Safe Design.	8
Unit 5	**Design for Testability:** Testability, Controllability and Observability, Design of Testable Combinational Logic Circuits, Testable Design of Sequential Circuits, Scan Path Techniques for Testable sequential circuits design, Level Sensitive Scan Design, Random Access Scan Techniques, Built in Test, Design Testability into Logic Boards.	8

Course Learning Outcomes (CLO):
Upon Completion of the topics

1. To explain the concept of reliability & faults in digital circuit.
2. Understand the design, testing & fault tolerant design.

Text Books:

1. Fault Tolerant and Fault Testable Hardware Design by P. K. Lala , BS publication.
2. *Digital circuits* and *logic design, Samuel C. Lee*, by PHI.
3. Diraj K. Pradhan, "Fault Tolerant Computer System Design", Prentice Hall.

Reference Books:

4. M. Abramovici, M.A. Breuer, A.D. Friedman, "Digital systems testing and testable design", Jaico Publishing House.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	3					3		3	
2	1	3	2		1			2		2	2

MECPE 203: ARTIFICIAL NEURAL NETWORK

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. understand explain strengths and weaknesses of the neural-network algorithms
2. Determine under which circumstances neural networks are useful in real applications
3. distinguish between supervised and unsupervised learning and explain the key principles of the corresponding algorithms

Unit	Topic	No. of Lecture
Unit 1	Introduction: Biological Neural Networks, Characteristics of Neural Networks, Models of Neuron, Basic Learning Rules, Stability & Convergence. Supervised Learning Neural Networks, Adaptive networks, Adaline and madaline, Single layer and multi layer perceptrons Radial basis function networks, Modular neural networks.	**9**
Unit 2	Feedback Neural Networks, Analysis of linear auto adaptive feed forward networks, Analysis of pattern storage Networks, Stochastic Networks & Stimulated Annealing, Boltzman machine. Unsupervised Learning Networks, Competitive learning, Kohonen self-organizing maps, learning vector quantization Principal component analysis of Hebbian Learning, Adaptive Resonance Theory.	**10**
Unit 3	Architectures for Pattern Recognition, Associative memory, Pattern mapping, Stability – Plasticity dilemma, ART, temporal patterns, Pattern visibility: Neocognitron.	**7**
Unit 4	Applications of Neural Networks, Pattern classification, Associative memories, Optimization, Applications in Image Processing, Applications in decision making	**7**
Unit 5	Fuzzy Set Theory Introduction to Fuzzy Set with Properties, Fuzzy Relations, Fuzzy Arithmetic, Fuzzy Logic, Applications and Fuzzy Control.	**7**

Course Learning Outcomes (CLO):

1. understand neural network(NN) paradigms
2. learn fuzzy logic
3. have a knowledge of evolutionary computations, genetic algorithm(GA), evolutionary programming, classifier systems, genetic programming parse trees, mathematical foundation of GA variants of GA
4. efficiently and reliably implement the artificial algorithm and engineering problems,
5. Describe principles of more general optimization algorithms.

Text Books:

1. B. Yegnanarayana, "Artificial Neural Networks", PHI.
2. James A Freeman, David M Skapura, "Neural Networks-Algorithm s, Applications and Programming Techniques," Person Education.
3. S. N. Sivanandam, S. Sumathi, S. N. Deepa, "Introduction to Neural Networks Using MATLAB 6.0" TMH Publication.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2		2	2					2	
2		2			2		3			2	2
3	3	3	2	1							
4				2	3				1		
5	3	2	1	2						1	1

MECOE 101: DESIGN OF DIGITAL IC

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet with the objectives of

1. To understand the basics of MOS in different regions of operation and to understand how to apply proper bias voltages so as to operate as a switch or amplifier.
2. To understand the operations of CAD tools in the design and analysis of MOS circuits.

Unit	Topic	No. of Lecture
Unit I	Basic Electrical Properties of MOS circuits: MOS transistor operation in linear and saturated regions, MOS transistor threshold voltage, MOS switch and inverter, latch-up in CMOS inverter; sheet resistance and area capacitances of layers, wiring capacitances;	**7**
Unit II	CMOS inverter properties - robustness, dynamic performance, regenerative property, inverter delay times, switching power dissipation, Combinational logic design in CMOS	**8**
Unit III	MOSFET scaling - constant-voltage and constant-field scaling; dynamic CMOS design: steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, NP-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme;	**8**
Unit IV	Subsystem design: design of arithmetic building blocks like adders - static, dynamic, Manchester carry-chain, look-ahead, linear and square-root carry-select, carry bypass and pipelined adders and multipliers - serial-parallel Braun, Baugh-Wooley and systolic array multipliers, barrel and logarithmic shifters, area-time tradeoff, power consumption issues;.	**7**
Unit V	Designing semiconductor memory and array structures: memory core and memory peripheral circuitry. Virtual and high speed memory design. Custom cell based design. Digital circuit testing and testability	**10**

Course Learning Outcomes (CLO):

Upon Completion of the topics:

1. Students will be able to bias MOS transistors depending on requirements.
2. Understand the basic Physics and Modelling of MOSFETs.
3. Knowledge about operations of MOS circuits.

Text Books:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation" John Wiley & Sons.

Reference Books:

2. U. Meyer -Baese, "Digital Signal Processing with Field Programmable Gate Arrays" Springer.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2	2					1		
2	3		2						1		
3	3	2	2								

MECOE 102: MICRO-CONTROLLER BASED SYSTEM DESIGN

Course Objectives:

L	T	P	CR
3	1	0	4

The course is designed to meet the objectives of:

1. The ambitious students, from the school of technology, a platform to build and materialize their original ideas into
2. Purely practical or project based in which the emphasis would be given on application of microcontrollers, logic families, ROM, etc. in designing an embedded system based product.

Unit	Topic	No. of Lecture
Unit I	Introduction to embedded systems – hardware and software components –types- examples characteristics –system on chip-challenges in embedded computing system design – embedded system design process. Various logic families, features, comparison, PLA, PAL, GAL, comparison, combinational PAL, PAL, FPGA, and Gate Arrays	6
Unit II	Embedded C compiler, advantages, memory models, interrupt functions, code optimization, 89C2051 micro-controller- architecture, comparison with 89C51, design of a simple trainer circuit using 89C51/89C2051 µC, interfacing of DIP switch, LED, 7 segment display, alphanumeric LCD, relay interface, design of a traffic light control system, interfacing programs using C and assembly language.	**8**
Unit III	Analog to digital converters, single slope, dual slope, successive approximation, sigma delta, flash, comparison, typical ICs, A/D interface, digital to analog converters, different types, D/A interface, optically isolated triac interface, design of a temperature control system, interfacing programs using C and assembly language.	**8**
Unit IV	Serial bus standards, I2C bus, SPI bus, operation, timing diagrams, 2 wire serial EEPROM, 24C04, 3wire serial EEPROM, 93C46, interfacing, serial communication standards, RS232, RS422, RS485, comparison, MAX232 line driver/ receiver , interfacing, interfacing programs using C and assembly language, low voltage differential signaling, PC printer port, registers, interfacing, universal serial bus, PCI bus.	**9**
Unit V	Matrix key board interface, AT keyboard, commands, keyboard response codes, watch dog timers, DS1232 watch dog timer, real time clocks, DS1302 RTC, interfacing ,measurement of frequency, phase angle, power factor, stepper motor interface, dc motor speed control, L293 motor driver, design of a position control system, interfacing programs using C and assembly language.	**9**

Course Learning Outcomes (CLO):

Upon Completion of the topics students able to

1. Explain the design of logic families.
2. Explain the coding of microcontroller using C language.

Text/Reference Books:

1. The 8051 Microcontroller: Muhammad Ali Mazidi, Pearson Education.
2. The 8051 Microcontroller: Kenneth J Ayala, Penram International.
3. Digital fundamentals: Floyd, Pearson Education.
4. Programming and customizing the 8051 μC: Myke Predko, TMH.
5. Programming with ANSI C and turbo C: Kamthane, Pearson Education.
6. Microcomputers and Microprocessors: John Uffenbeck, PH

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2	2					1		
2	3		2						1		2

MECPE 402: ADVANCE COMPUTER ARCHITECTURE

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. Technical competence in computer architecture and high performance computing.
2. Development of software to solve computationally intensive problems.

Unit	Topic	No. of Lecture
Unit I	Instruction level parallelism ILP- Concepts and challenges, Hardware and software approaches, Dynamic scheduling, Speculation Compiler techniques for exposing ILP, Branch prediction.	7
Unit II	Multiple issue processors vliw & epic, Advanced compiler support, Hardware support for exposing parallelism, Hardware versus software speculation mechanisms, IA 64 and Itanium processors, Limits on ILP.	**8**
Unit III	Multiprocessors and thread level parallelism Symmetric and distributed shared memory architectures, performance issues synchronization, models of memory consistency, introduction to multithreading.	**9**
Unit IV	Memory and i/o Cache performance, Reducing cache miss penalty and miss rate, Reducing hit time Main memory and performance, Memory technology. Types of storage devices, Buses, RAID, Reliability, availability and dependability, I/O performance measures, Designing an I/O system.	**8**
Unit V	Multi-core architectures, Software and hardware multithreading, SMT and CMP architectures, Design issues, Case studies, Intel Multi-core architecture, SUN CMP architecture, heterogeneous, multi-core processors , case study: IBM Cell Processor.	**8**

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Course Learning Outcomes (CLO):

Upon Completion of the topics students able to

1. Describe the principles of computer design.
2. Classify instruction set architectures.
3. Describe the operation of performance enhancements such as pipelines, dynamic scheduling, branch prediction, caches, and vector processors.

Text Books:

1. John L. Hennessey and David A. Patterson, "Computer architecture – A quantitative Approach, MK publication Elsevier.

Reference Books:

2. Kai Hwang and Zhi.Wei Xu, "Scalable Parallel Computing", Tata McGraw Hill, T. Cormen, C. Leiserson and R. A. Rivest, Algorithms, MIT Press and McGraw-Hill.
3. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture "A Hardware/ software approach" , Morgan Kaufmann /Elsevier Publishers.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2	2					1		
2		3		3					1		2
3		3		3						2	

MECPE 403: PATTERN RECOGNITION

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. This course will serve as a comprehensive introduction to various topics in machine learning.

Unit	Topic	No. of Lecture
Unit I	**Introduction:** Basics of pattern recognition, Design principles of pattern recognition system, Learning and adaptation, Pattern recognition approaches, Mathematical foundations – Linear algebra, Probability Theory, Expectation, mean and covariance, Normal distribution, multivariate normal densities, Chi squared test.	**8**
Unit II	**Statistical Patten Recognition:** Bayesian Decision Theory, Classifiers, Normal density and discriminant functions.	**8**
Unit III	**Parameter Estimation Methods:** Maximum-Likelihood estimation, Bayesian Parameter estimation, Dimension reduction methods - Principal Component Analysis (PCA), Fisher Linear discriminant analysis, Expectation-maximization (EM), Hidden Markov Models (HMM), Gaussian mixture models.	**7**
Unit IV	**Nonparametric Techniques:** Density Estimation, Parzen Windows, K-Nearest Neighbor Estimation, Nearest Neighbor Rule, Fuzzy classification.	**10**
Unit V	**Unsupervised Learning & Clustering:** Criterion functions for clustering, Clustering Techniques: Iterative square - error partitional clustering – Kmeans, agglomerative hierarchical clustering, Cluster validation.	**7**

Course Learning Outcomes (CLO):

Upon Completion of the topics students able to

1. Design and implement machine learning solutions to classification, regression, and clustering problems.
2. Evaluate and interpret the results of the algorithms.

Reference Books:

1. Richard O. Duda, Peter E. Hart and David G. Stork, "Pattern Classification", 2ndEdition, John Wiley, 2006.
2. C. M. Bishop, "Pattern Recognition and Machine Learning", Springer, 2009.
3. S. Theodoridis and K. Koutroumbas, "Pattern Recognition", 4thEdition, Academic Press.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2	2					1		
2		3		3					1		2

MECOE 104: COMPOUND SEMICONDUCTORS

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. Making the students to study the characteristics of compound semiconductor.
2. Making student to understand the future of compound semiconductor.

Unit	Topic	No. of Lecture
Unit 1	Structure, bonding and ionicity of compound semiconductors, binary and ternary alloy systems; phase diagrams - Ga-As, InP, CdTe, and HgCdTe systems; stoichiometry and composition of IIIV and II-V compounds, Charge transport, lattice modes and scattering processes, ionized impurity, acoustic, piezoelectric and polar optical scattering, quantum effects - 2 dimensional transport	**10**
Unit 2	quantum hall effect, super lattices, resonant tunneling, transport in presence of magnetic fields, Gunn effect, impact ionization and avalanche breakdown, Optical absorption and emission, band structure, dependence on temperature, pressure, composition and degeneracy, impurity and free carrier absorption.	**9**
Unit 3	electrons at heterojunctions, electrons in nanostructures, electrons in coupled nanostructures, photons	**7**
Unit 4	substrates and epitaxy, thin films, device processing, electronics, in-plane optoelectronics, out-of-plane optoelectronics	**7**
Unit 5	magneto-optical effects, luminescence, heterojunctions and interfaces, growth and process induced defects, deep levels, persistent photoconductivity, Applications of compound semiconductors as sensors and actuators.	**7**

Course Learning Outcomes (CLO):

1. Clear understanding & application of compound semiconductor.
2. To explain the concept of optoelectronic devices.

Text Books:

1. World of Compound semiconductor.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2	2						2	1
2		3		3							2

MECPD 101: DISSERTATION-I

L	T	P	CR
0	0	8	7

Students have to perform a mini project work related to their respective stream in M. Tech. The project work may be software or hardware based. /it may be extendable to major project in next semester.

Course Learning Outcomes (CLO):
Students successfully completing this module will be able to:

1. Understand advanced topics in microelectronic & VLSI design.
2. Implement a mini project based on hardware & software or may be a part of major project.
3. Improve language and communication skills.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1				3	3		2				
2				3	3		3			2	3
3						3					

MECPD 102: DISSERTATION-II

L	T	P	CR
0	0	8	7

Students have to perform a mini project work related to their respective stream in M. Tech. The project work may be software or hardware based. /it may be extendable to major project in next semester.

Course Learning Outcomes (CLO):

Students successfully completing this module will be able to:

1. Understand advanced topics in microelectronic & VLSI design.
2. Implement a mini project based on hardware & software or may be a part of major project.
3. Improve language and communication skills.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1				3	3		2				
2				3	3		3			2	3
3						3					

MECPE 204: NANO TECHNOLOGY

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives:

1. To introduce students with diversified backgrounds to the expanding nano-world.
2. Lecture and Web-based learning supplemented class materials to increase exposure to students and bring material forward for discussion.
3. To effectively encouraged not only students but local professionals to participate in design proposals and to pursue further nanotechnology studies.

Unit	Topic	No. of Lecture
Unit I	Introduction, science behind nanotechnology, bio systems, molecular recognition, quantum mechanics & quantum ideas, optics. Smart materials & Sensors, self healing structures	**7**
Unit II	Heterogeneous nano structures & composites, encapsulations, natural nanoscale sensors, electromagnetic sensors, biosensors, electronic noses.	**8**
Unit III	Nanostructures, Micro/Nanodevices, Nanomaterials Synthesis and Applications, Molecule-Based Devices- Introduction to Carbon Nanotubes, Nanowires	**8**
Unit IV	Introduction to Micro/Nanofabrication.- Stamping Techniques. Methods and Applications. Materials Aspects of Micro- and Nanoelectromechanical Systems- MEMS/NEMS Devices and Applications, Nanodevices, Scanning Probe Microscopy	**7**
Unit V	Noncontact Atomic Force Microscopy and Its Related Topics - Low Temperature Scanning Probe Microscopy, Dynamic Force Microscopy- Nanolithography, Lithography using photons, electron beams soft lithography, Bio- medical applications.	**10**

Course Learning Outcomes (CLO):

1. To demonstrate the ease of application and progression of integrating nanotechnology into the undergraduate education curriculum for engineering students, while providing hands on learning and initial research experience.
2. This coursework demonstrates substantial opportunities for students and faculty, while bringing forth the nanotechnology paradigm shift opportunities to the masses.

Text/Reference Books:

1. Mark Ratner, Daniel Rattner, "Nanotechnology: A Gentle Introduction to the Next Big Idea", Pearson Education.
2. Nanotechnology :Principals &practices, Sulbha K. Kulkarni, Capital publishing company, ISBN:-
   81-85589-29-1.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3			2				3	3	3	
2	3	2			1			2	3	2	2

MECPE 302: MEMORY TECHNOLOGIES

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. to make the students to build a solid foundation about different type of RAM.
2. to make the students to study Digital Logic Gates and Circuits
3. to provide a clear foundation of Modern Digital Display devices.

Unit	Topic	No. of Lecture
Unit I	Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar, SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies- Application Specific SRAMs.	**7**
Unit II	DRAMs, DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP.	**8**
Unit III	EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application.	**9**
Unit IV	Specific Memory Testing. General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.	**8**
Unit V	Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories(MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.	**8**

Course Learning Outcomes (CLO):

1. clear understanding & utilization of RAM
2. design and develop of advanced RAM circuits
3. utilization of Combinational and Sequential circuits.

Text/Reference Books:

1. Ashok K. Sharma, " Semiconductor Memories Technology, Testing and Reliability ".Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Manish Verma and Peter Marwedel "Advance Memory optimization techniques for Low Power Embedded processors", Springer Publication.
3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2							2	3	1
2	3				1				3	2	2
3	2	2	2							2	2

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MECPE104: CAD OF VLSI DESIGN

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. To provide an introduction to the fundamentals of Computer-Aided Design tools for the modeling, design, analysis & test.
2. Verification of digital Very Large Scale Integration (VLSI) systems.

Unit	Topic	No. of Lecture
Unit I	**VLSI DESIGN METHODOLOGIES:** Introduction to VLSI Design methodologies, Review of Data structures and algorithms, Review of VLSI Design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, general purpose methods for combinatorial optimization.	**8**
Unit II	**DESIGN RULES:** Layout Compaction, Design rules, problem formulation, algorithms for constraint graph compaction, placement and partitioning, Circuit representation, Placement algorithms, partitioning	**8**
Unit III	**FLOOR PLANNING:** Floor planning concepts, shape functions and floor-plan sizing, Types of local routing problems, Area routing, channel routing, global routing, algorithms for global routing.	**7**
Unit IV	**SIMULATION:** Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.	**9**
Unit V	**MODELLING AND SYNTHESIS:** High level Synthesis, Hardware models, Internal representation, Allocation assignment and scheduling, Simple scheduling algorithm, Assignment problem, High level transformations.	**8**

Course Learning Outcomes (CLO):

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD.
3. Demonstrate knowledge of computational and optimization algorithms and tools applicable to solving CAD related problems.
4. Establish capability for CAD tool development and enhancement.

Text Books:

1. K. Hoffman and R.E. Kunze, Linear Algebra, Prentice Hall (India).

Reference Books:

2. N. Balabanian and T.A. Bickart, Linear Network Theory: Analysis, Properties, Design and Synthesis, Matrix Publishers.
3. T. Cormen, C. Leiserson and R. A. Rivest, Algorithms, MIT Press and McGraw-Hill.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3							3	3	3	
2	3				1			2	3	2	2
3	2	2			2						1
4	3	2	1						3	2	

MECPE 303: ARTIFICIAL INTELLIGENCE

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

3. To introduce the fundamental concepts of artificial intelligence;
4. To equip students with the knowledge and skills in logic programming using Prolog;
5. To explore the different paradigms in knowledge representation and reasoning;
6. To understand the contemporary techniques in machine learning;
7. To evaluate the effectiveness of hybridization of different artificial intelligence techniques.

Unit	Topic	No. of Lecture
Unit 1	Introduction to Artificial Intelligence Definition, AI Applications, AI representations, properties of internal representations Heuristic Search Techniques, Best File Search, Mean and End Analysis, A* and AO* Algorithms.	**9**
Unit 2	Neural Networks, Learning by training neural networks, Introduction to neural net works, Neural net architecture & applications, Natural language processing & understanding & paragmatic, Syntactic, Semantic, Qualities, finite state machines, RTN, ATN, understanding sentences.	**8**
Unit 3	Game Playing & Predicate Logic Minimax search procedure, Alpha-beta cut-offs, Waiting for Quiescence, Secondary Search, Predicate Calculus, Predicate and arguments, ISA Hierarchy, Frame Notation, Resolution, Natural Deduction.	**8**
Unit 4	Knowledge Representation Using Non-Monotonic Logic Truth Maintenance System, Statistical and Probabilistic Reasoning, Semantic-net Frames, Script, Conceptual Dependency.	**7**
Unit 5	Planning Block world, strips, Implementation using goal stack, Non-linear planning using goal stacks, Hierarchical planning, List commitment strategy. Expert Systems Utilization and functionality, Architecture of expert systems, Knowledge representation, Two case studies on expert systems.	**8**

Course Learning Outcomes (CLO):

1. understand the history, development and various applications of artificial intelligence;
2. familiarize with propositional and predicate logic and their roles in logic programming;
3. understand the programming language Prolog and write programs in declarative programming style;
4. master the skills and techniques in machine learning, such as decision tree induction, artificial neural networks, and genetic algorithm;

Reference Books/Text Books:

1. Ela Kumar, "Artificial Intelligence" I. K. International.
2. Rajendra Akerkar, "Introduction to Artificial Intelligence" PHI
3. K. Uma Rao, "Artificial Intelligence and Neural Network", Pearson Publication
4. Eugane. Charniak, Drew McDermott, "Introduction to Artificial Intelligence", Pearson Education.
5. Kishan Mehrotra, Sanjay Rawika, K. Mohan, "Artificial Neural Network" .
6. Rajendra Akerkar, "Introduction to Artificial Intelligence", Prentice Hall Publication.
7. S. N. Sivanandam, S. Sumathi, S. N. Deepa, "Introduction to Neural Networks Using MATLAB" TMH Publication.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2						3	3	
2	3	2							3	2	2

OK

MECOE 102: MICRO ELECTRO MECHANICAL SYSTEM

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. Introduction to MEMS and micro fabrication
2. To study the essential material properties.
3. To study various sensing and transduction technique.
4. To know various fabrication and machining process of MEMS.
5. To know about the polymer and optical MEMS.

Unit	Topic	No. of Lecture
Unit 1	**INTRODUCTION TO MICROSYSTEMS:** Review of microelectronics manufacture and introduction to MEMS Overview of Microsystems technology. Laws of scaling. The multi disciplinary nature of MEMS. Survey of materials central to micro engineering. Applications of MEMS in various industries.	**9**
Unit 2	**MICRO MANUFACTURING TECHNIQUES:** Photolithography, Film deposition, Etching processes, Bulk micro machining, silicon surface micro machining, LIGA process, Rapid micro product development.	**8**
Unit 3	**MICRO SENSORS AND MICRO ACTUATORS:** Energy conversion and force generation, Electromagnetic Actuators, Reluctance motors, piezoelectric actuators, bi-metal-actuator Friction and wear. Transducer principles, Signal detection and signal processing, Mechanical and physical sensors, Acceleration sensor, pressure sensor, Sensor arrays.	**9**
Unit 4	**INTRODUCTION TO MICRO / NANO FLUIDS:** Fundamentals of micro fluidics, Micro pump – introduction – Types – Mechanical Micro pump – Non Mechanical micro pumps, Actuating Principles, Design rules for micro pump – modeling and Simulation , Verification and testing – Applications.	**7**
Unit 5	**MICROSYSTEMS DESIGN AND PACKAGING:** Design considerations, Mechanical Design, Process design, Realization of MEMS components using intellisuite. Micro system packaging, Packing Technologies, Assembly of Microsystems, Reliability in MEMS.	**7**

Course Learning Outcomes (CLO):

1. Be familiar with the important concepts applicable to MEMS, their fabrication.
2. Be fluent with the design, analysis and testing of MEMS.
3. Apply the MEMS for different applications.

Text Books:

1. Mohamed Gad – el – Hak , MEMS Handbook, CRC Press, 2002.
2. Rai-Choudhury P, MEMS and MOEMS Technology and Applications, PHI Learning Private Limited, 2009.

Reference Books:

3. Sabrie Solomon, Sensors Handbook, Mc Graw Hill, 1998.
4. Marc F Madou, Fundamentals of Micro Fabrication, CRC Press, 2nd Edition, 2002.
5. Francis E.H. Tay and W.O. Choong , Micro fluidics and Bio mems application, IEEE Press New York, 1997.
6. Trimmer William S., Ed., Micromachanics and MEMS, IEEE Press New York, 1997.
7. Maluf, Nadim, An introduction to Micro electro mechanical Systems Engineering, AR Tech house, Boston 2000.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2					3	2	3	
2	3		2					2	3	2	2
3		3	2						2	2	

MECOE 103: Information Security

L	T	P	CR
3	1	0	4

Course Objectives:

The course is designed to meet the objectives of:

1. Introducing basic concepts of information security, web security & database security that we use in our day-to-day life.
2. To have clear understanding of various 3GPP concepts and non 3GPP.

Unit	Topic	No. of Lecture
Unit I	**Information Security:** Attacks on information, components of Information Security, Cryptographic techniques, public & private key, mathematical tools of cryptography, Cryptography techniques, Authentication access control, Digital signature, Certificates & standards.	**9**
Unit II	**Cypher Algorithm:** Design principles of block ciphers & Block Cipher Algorithms, Electronic mail security, RSA algorithm, MD5, IDEA, RC2, RC5 algorithm, Stenography techniques.	**8**
Unit III	**Web Security:** SSL protocol security, HTTPS, WTLS protocol in WAP, Introduction to Web based bio AuC, issues of s/w piracy & copyright, Introduction to IT act 2000.	**7**
Unit IV	**Mobile Attacks:** 3 GPP security, Mobile Virtual Private n/w, Smart Card security, RFID security, Mobile Agent security, Mobile virus, mobile worms	**8**
Unit V	**Database Security Systems:** Network security concept, Trojans, Intrusion detection, Firewall, Cyber law related to E-commerce.	**8**

Course Learning Outcomes (CLO):

1. Understand the design and develop different aspects of information & web security.
2. Understand various 3GPP based system and Non 3GPP systems.

Reference Books:

1. Stallings, William- "Cryptography & Network Security: principle and Practices" Pearson Education.
2. Asoke K Talukder, Hasan Ahamad, Roopa R Yavagal "Mobile Computing" TMH Publication.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	2					3		3	
2	3		2		2			2	3	2	

MECPD 103: DISSERTATION-III

L	T	P	CR
0	0	24	16

The project/dissertation shall be finalized by the students based on the VI semester project/dissertation work report and shall be completed and submitted at least one month before date of which shall be notified in the academic calendar.

The assessment of performance of students should be made at least twice in VI semester. In this semester student shall present the final project live as also using overheads project or power point presentation on LCD to the internal committee as also the external examiner.
The evaluation committee shall consist of faculty members constituted by the Institution which would comprise of at-least three members comprising of the HOD, project/ dissertation guide and a nominee of the Dean. The students guide would be a special invitee to the presentation. The seminar session shall be an open house session. The internal marks would be the average of the marks given by each member of the committee separately in a sealed envelope to the HOD.

Course Learning Outcomes (CLO):

Students successfully completing this module will be able to:

1. Recognize and formulate a problem to analyze, synthesize, evaluate, simulate and create a power electronic converter and/or a drive system.
2. Carryout modeling and simulation studies pertaining to the system and prepare a presentation.
3. Build the hardware to demonstrate the principle of working.
4. Correlate the analytical, simulation and experimental results.
5. Deduce conclusions and draw inferences worthy of publication.

MAPPING OF CLO WITH PO

Course Learning Outcomes (CLO):	Program Outcomes(PO)										
	1	2	3	4	5	6	7	8	9	10	11
1	3	2	3	3	1						
2	2				2	3					
3						2	3			3	
4							3	2	1	2	2
5					3	2	1			3	