Rama University Uttar Pradesh, Kanpur
Faculty of Engineering & Technology

Ref: RU/FET/ECE/BOS/2014/001 **Dated: 28/04/2014**

Faculty of Engineering & Technology
Department of Electronics & Communication Engineering
Minutes of Meeting
Boards of Studies

A meeting of Boards of Studies of Electronics & Communication Engineering, FET was held on 26/04/2014 (Saturday) at 2:30 PM. in conference room of FET. The following members were present:

1. Dr. Harish Kumar - Chairperson
2. Mr.Ravi Dixit - Member
3. Mr.Deepak Patel - Member

The following members agreed to review the minutes in Delhi.

1. Prof. Manoj Shukla - External Member
2. Mr. Surya Prakash Tiwari - External Member

Agenda:

1. Action Taken Report (ATR) on the basis of feedback from Stack holder/External member

The department teams have been working on the curricula and syllabus and consider their feedback and suggestion of stack holder/External member. They suggested that the focus must be on fundamental and practical courses having emphasis on research and development.

Action taken: Courses like (i) Semiconductor of Device Modeling (ii) Architectural Design of ICs (iii) Digital VLSI Circuit (iv) Nano Technology.

2. To review the Vision and Mission statements of the newly established of Electronics & Communication Engineering Department.

The Board of Studies reviewed the Vision and Mission statements prepared by the HoD, ECE. The Board suggested minor revisions in the both the statements and recommends the final draft for adoption by the Academic Council.

Attached revised Vision and Mission statements in Annexure: **1**.

3. **To review the Program Outcomes (PO), Program Specific Outcomes (PSO) and Program Educational Objectives (PEO) for M.Tech program**.

The Board reviewed the Program Outcomes (POs) for M.Tech. Program and revised them to fit into the Frame work laid down by the National Board of Accreditation.

The Program Specific Outcomes (PSO) and Program Educational Objectives (PEO) for M.Tech. Program were reviewed and recommended for approval by the Academic Council.

(Annexure 2 & 3)

Rama University Uttar Pradesh, Kanpur
Faculty of Engineering & Technology

4. To consider and approved the curricula and syllabus.

S. No.	Item No.	Existing	Recommendation /Action Taken
1	To conceder and recommendation the evaluation scheme & syllabus for M.Tech students admitted in the session 2014-15.	....	The BOS consider the curricula and syllabus and discuss the credit of each subjects should be added in detailed syllabus of every subject. The BOS recommended the curricula and syllabus for approval by the Academic Council. **(Annexure 4)**

The meeting concluded with a vote of thanks to the chair.
Date of the Next Meeting: to be decided and conveyed later

(Chairman)

Annexure:

1. Vision and Mission Statement for Department of Electronics & Communication Engineering
2. Program Outcomes (PO) for M.Tech Program
3. Program Specific Outcomes (PSO) & Program Educational Objectives (PEO) for M.Tech. Program
4. Evaluation Scheme & Syllabus

CC:
1. Dean
2. Registrar Office

Study &Evaluation Scheme

Master of Technology

(Electronic & Communication Engineering)

[Applicable w.e.f Academic Session 2014-15 till revised]

FACULTY OF ENGINEERING &TECHNOLOGY

RAMA UNIVERSITY, UTTAR PRADESH, KANPUR

Website: www.ramauniversity.ac.in

RAMA UNIVERSITY UTTAR PRADESH, KANPUR

A meeting of the Board of Studies of the department of M.Tech Microelectronic & VLSI Design of Faculty of Engineering and Technology Rama University Uttar Pradesh, Kanpur was held on 16th June 2014 at 11 AM. The following members were present:

1. Dr. Harish Kumar	Convener
2. Mr.Ravi Dixit	Member
3. Mr.Deepak Patel	Member
4. Prof. Manoj Shukla	External Member
5. Mr. Surya Prakash Tiwari	External Member

The quorum of the meeting was complete.

Agenda of the meeting:

1. Assessment Criteria
2. Question Paper Format
3. Syllabus

The meeting resolved unanimously that attached Assessment Criteria, Question Paper Format and Syllabus are justified and approved.

Convener

Signature: .....
Name : Dr. Harish Kumar
Date:

Internal Members

Signature: 1..... 2.....
Name: Mr.Ravi Dixit Mr.Deepak Patel
Date:

External Members

Signature: 1..... 2.....
Name: Prof. Manoj Shukla Mr. Surya Prakash Tiwari
Date:

Rama University Uttar Pradesh, Kanpur

Faculty of Engineering and Technology
Course Detail and Evaluation Scheme
(Effective from the Session 2014-15)
M. Tech. – Microelectronics and VLSI Design

YEAR 1st , SEMESTER-I

S. No.	Course Code	SUBJECT	PERIODS			EVALUATION SCHEME			Subject Total	Credit
			L	T	P	CE	MTE	ETE		
THEORY SUBJECTS										
1.	MEC101	Semiconductor Device Modeling	3	1	0	20	20	60	100	4
2.	MEC102	Architectural Design of ICs	3	1	0	20	20	60	100	4
3.	MEC103	Analog VLSI Design	3	1	0	20	20	60	100	4
4.	MEC104	VLSI Technology	3	1	0	20	20	60	100	4
PRACTICAL										
5.	MEC151	VLSI Design Lab	0	0	4	30	20	50	100	2
6	MEC152	Memory Technologies	0	0	4	30	20	50	100	2
		Total	**12**	**4**	**8**	**140**	**120**	**340**	**600**	**20**

L-Lecture, T-Tutorial, P- Practical, CE- Continuous Evaluation, MTE-Mid Term Examination, ETE-End Term Examination

Evaluation Scheme:

- **Course without practical components**

For Continuous Evaluation (CE) is such as: 20 Marks

1. Attendance: 5 Marks
2. Assignments/ Quiz / Seminar/Term paper /Project :15Marks

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 60 Marks

- **Course with practical components only**

For Continuous Evaluation (CE) is such as: 30 Marks
Conduct / Perform/Execution /Practical File/ Viva-Voice

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 50 Marks

Rama University Uttar Pradesh, Kanpur

Faculty of Engineering and Technology
Course Detail and Evaluation Scheme
(Effective from the Session 2014-15)
M. Tech. – Microelectronics and VLSI Design

YEAR 1st, SEMESTER-II

S. No.	Course Code	SUBJECT	PERIODS			Evaluation Scheme			Subject Total	Credit
			L	T	P	CE	MTE	ETE		
	THEORY SUBJECTS									
1.	MEC 201	Digital VLSI Circuit	3	1	0	20	20	60	100	4
2.	MEC 202	Advance Microprocessor & Microcontroller	3	1	0	20	20	60	100	4
3.	MEC 203	Low Power VLSI Design	3	1	0	20	20	60	100	4
4.	MEC 011-014	Departmental Elective I	3	1	0	20	20	60	100	4
	PRACTICAL									
5.	MEC251	VLSI CAD Lab	0	0	4	30	20	50	100	2
6	MEC252	Advance Microprocessor & Microcontroller Lab	0	0	4	30	20	50	100	2
		Total	**12**	**4**	**8**	**140**	**120**	**340**	**600**	**20**

L-Lecture, T-Tutorial, P- Practical, CE- Continuous Evaluation, MTE-Mid Term Examination, ETE-End Term Examination

Evaluation Scheme:

- **Course without practical components**

For Continuous Evaluation (CE) is such as: 20 Marks

3. Attendance: 5 Marks
4. Assignments/ Quiz / Seminar/Term paper /Project :15Marks

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 60 Marks

- **Course with practical components only**

For Continuous Evaluation (CE) is such as: 30 Marks
Conduct / Perform/Execution /Practical File/ Viva-Voice

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 mar

ETE - End Term Examination: 50 Marks

Rama University Uttar Pradesh, Kanpur

Faculty of Engineering and Technology
Course Detail and Evaluation Scheme
(Effective from the Session 2014-15)
M. Tech. – Microelectronics and VLSI Design

YEAR 2nd, SEMESTER-III

S. No.	Course Code	SUBJECTS	PERIODS			Evaluation Scheme			Subject	Credit
			L	T	P	CE	MTE	ETE		
THEORY SUBJECTS										
1.	MEC 021-026	Departmental Elective II	3	1	0	20	20	60	100	4
2.	MEC 031-036	Departmental Elective III	3	1	0	20	20	60	100	4
PROJECT										
3.	MEC 351	Dissertation I	0	0	16	200	00	300	500	12
		Total	**6**	**2**	**16**	**240**	**40**	**420**	**700**	**20**

L-Lecture, T-Tutorial, P- Practical, CE- Continuous Evaluation, MTE-Mid Term Examination, ETE-End Term Examination

Evaluation Scheme:

- **Course without practical components**

For Continuous Evaluation (CE) is such as: 20 Marks

5. Attendance: 5 Marks
6. Assignments/ Quiz / Seminar/Term paper /Project :15Marks

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 60 Marks

- **Course with practical components only**

For Continuous Evaluation (CE) is such as: 200 Marks
Conduct / Perform/Execution /Practical File/ Viva-Voice/ Dissertation

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 50 Marks

Rama University Uttar Pradesh, Kanpur

Faculty of Engineering and Technology
Course Detail and Evaluation Scheme
(Effective from the Session 2014-15)
M. Tech. – Microelectronics and VLSI Design

YEAR 2nd, SEMESTER-IV

S. No.	Course Code	SUBJECT	PERIODS			Evaluation Scheme			Total Marks	Credit
			L	T	P	CE	MTE	ETE		
THEORY SUBJECTS										
1.	MEC451	Dissertation II	0	0	24	300	00	400	700	20
		Total	**0**	**0**	**24**	**300**	**00**	**400**	**700**	**20**

L-Lecture, T-Tutorial, P- Practical, CE- Continuous Evaluation, MTE-Mid Term Examination, ETE-End Term Examination

Evaluation Scheme:

- **Course without practical components**

For Continuous Evaluation (CE) is such as: 20 Marks

7. Attendance: 5 Marks
8. Assignments/ Quiz / Seminar/Term paper /Project :15Marks

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 60 Marks

- **Course with practical components only**

For Continuous Evaluation (CE) is such as: 300 Marks
Conduct / Perform/Execution /Practical File/ Viva-Voice/ Dissertation

MTE - Mid Term Examination: 20 Marks

a. First Mid Term Examination: 10 marks
b. Second Mid Term Examination: 10 marks

ETE - End Term Examination: 50 Marks

Ravi Deepak

Semester: 1st

Subject Name: Semiconductor Device Modeling

Course Code: MEC 101 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Review of semiconductor physics: Quantum foundation, Carrier scattering, high field effects; P- N junction diode modeling: Static model, Large signal model and SPICE models,	**8**
Unit II	BJT modeling: Ebers Moll, Static, large-signal, small- signal models. Gummel - Poon model. Temperature and area effects. Power BJT model, SPICE models, Limitations of GP model; Advanced Bipolar models: VBIC, HICUM and MEXTARM; MOS Transistors: LEVEL 1, LEVEL 2 ,LEVEL 3, BSIM, HISIMVEKV Models	**8**
Unit III	Threshold voltage modeling. Punch through. Carrier velocity modeling. Short channel effects. Channel length modulation. Barrier lowering, Hot carrier effects.	**8**
Unit IV	Mobility modeling, Model parameters; Analytical and Numerical modeling of BJT and MOS transistors:	**8**
Unit V	Introduction to various simulation techniques, Noise modeling; Modeling of hetero-structure devices.	**8**

Text Book:

1. Ben G Streetmen and Sanjay Kumar Benerjee, "Solid State Electronics Device" PHI publication.
2. Muller and Kamins, "Device Electronics for Integrated Circuits", John Welley and sons.

Reference Books:

1. Millman J. and Halkias .C., " Integrated Electronics ", Tata McGraw-Hill.
2. Robert L. Boylestad and Louis Nashelsky, 8th edn. PHI.
3. S. Salivahanan, et.al, "Electronic Devices and Circuits", TMH.
4. Floyd, Electronic Devices, Sixth edition, Pearson Education.
5. I.J. Nagrath, Electronics - Analog and Digital, PHI.

Semester: 1st

Subject Name: Architectural Design of ICs

Course Code: MEC 102 **L T P C**

3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Introduction: VLSI Design flow, general design methodologies; Mapping algorithms into Architectures: Signal flow graph, data dependences, data path synthesis, control structures, critical path and worst case timing analysis, concept of hierarchical system design;	**10**
Unit II	Hardware Description Languages: Basic concepts of hardware description languages, Hierarchy, modeling, Structural, Data-flow and Behavioral styles of hardware description, Syntax and Semantics of VHDL, Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Modules, nets and registers, • Concurrent and sequential constructs, Examples of design using VHDL & Verilog.	**8**
Unit III	Pipeline and parallel architectures: Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures	**9**
Unit IV	Control strategies: Hardware implementation of various control structures, VLIW architecture; Testable architecture: Controllability and observability, boundary scan and other such techniques, identifying fault locations, self reconfigurable fault tolerant structures.	**6**
Unit V	Data path elements: Data path design philosophies, fast adder, multiplier, driver etc., data path optimization, application specific combinatorial and sequential circuit design, CORDIC unit.	**7**

Text Book:

1. C.Y. Chang and S.M. Sze (Ed), ULSI Technology, McGraw Hill.
2. Digital circuits and logic design, Samuel C. Lee, PHI.
3. William I. Fletcher," An Engineering Approach to Digital Design", Prentice Hall India.
4. Hill & Peterson, "Switching Circuit & Logic Design", Wiley.
5. Charles H Roth Jr, "Digital System Design using VHDL", Thomson Learning, 2002.
6. Douglas L Perry, "VHDL: Programming by Example", TMH publication.
7. Jayram Bhaskar, "VHDL Primer", TMH Pub.
8. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing, Allentown, PA) 1998.

Reference books:

1. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall (NJ, USA), 1996.

Semester: 1st
Subject Name: Analog VLSI Design

Course Code: MEC 103 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**SINGLE STAGE AMPLIFIERS:** Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower cascocde and folded cascade configurations, differential amplifiers and current mirror configurations.	**8**
Unit II	**HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS:** Current mirrors, cascode stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers	**8**
Unit III	**FEEDBACK AND OPERATIONAL AMPLIFIERS:** Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.	**8**
Unit IV	**STABILITY AND FREQUENCY COMPENSATION:** General considerations, Multipolesystems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.	**8**
Unit V	**BANDGAP REFERENCES:** supply independent biasing, temperature independent references, PTAT currentgeneration, Constant-Gm Biasing.	**8**

Text Book:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill
2. Willey M.C. Sansen, "Analog Design Essentials", Springer.

Reference books:

1. Gray and Mayer "Analysis and Design of Analog Integrated circuit", Welly India.
2. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons, Inc.
3. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second edition, Oxford.

Semester: 1st
Subject Name: VLSI Technology

Course Code: MEC 104 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Semiconductor review and survey of IC processing Roadmap; Silicon crystal growth and wafer preparation;	**9**
Unit2	Unit Processes : Substrate cleaning , Oxidation ; Doping techniques: Diffusion, Ion implementation ;	**7**
Unit 3	Pattern transfer: mask making & different lithography techniques (optical, x-ray, E-Beam, Ion-Beam); Vacuum science & plasmas; Etching: Isotropy, anisotropy, selectivity, wet plasma, RIBE etc.;	**8**
Unit 4	Thin films: Physical deposition, evaporation and sputtering; Chemical Vapor Deposition: CVD, LPCVD, PECVD, MOCVD, MBE etc. ; Epitaxial growth; Lithography: optical, electron beam, X-ray etc.	**8**
Unit 5	Process integration: Device isolation technology (junction, dielectric, LOCOS, trench etc); Advances in Bipolar, MOS and BICMOS process technologies; A case study using process simulation tools.	**8**

Text Books:

1. C.Y. Chang and S.M. Sze (Ed), ULSI Technology, McGraw Hill.

Semester: 1st
Subject Name: VLSI Design Lab

Course Code: MEC 151 **L T P C**
0 0 4 2

Analog Design Flow

1. Design an Inverter with given specifications*, completing the design flow
2. Mentioned below:
    a. Draw the schematic and verify the following
        i) DC Analysis
        ii) Transient Analysis
    b. Draw the Layout and verify the DRC, ERC
    c. Check for LVS
    d. Extract RC and back annotate the same and verify the Design. Verify & Optimize for Time, Power and Area to the given constraint
3. Design the following circuits with given specifications*, completing the
4. Design flow mentioned below:
    a. Draw the schematic and verify the following
        i) DC Analysis
        ii) AC Analysis
        iii) Transient Analysis
    b. Draw the Layout and verify the DRC, ERC
    c. Check for LVS
    d. Extract RC and back annotate the same and verify the Design.
        i) AND, OR, NOR, NAND, XOR, XNOR with using of MOS technology.
5. Design the following circuits with given specifications*, completing the
6. Design flow mentioned below:
    a. Draw the schematic and verify the following
        i) DC Analysis
        ii) AC Analysis
        iii) Transient Analysis
    b. Draw the Layout and verify the DRC, ERC
    c. Check for LVS
    d. Extract RC and back annotate the same and verify the Design.
    e. Combinational circuit with using of MOS technology
7. Simulate a static CMOS circuit to compute f = (A+B) (C+D) with least each input can present a maximum of 30 lambda of transistor width. The output must drive a load equivalent to 500 lambda of transistor width. Choose transistor size to achieve least delay and estimate the delay in t.

Ram. Deepak

Semester: 1st
Subject Name: Logic Design Lab

Course Code: MEC 152 **L T P C**
0 0 4 2

1. HDL code to realize all the logic gates.
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
1. Look Ahead Adder.
2. Design and analysis of 4 bit binary to gray converter.
3. Design and analysis of Multiplexer/ Demultiplexer, comparator.
4. Design and analysis of Full adder using 3 modeling styles.
5. Design and analysis of flip flops: SR, D, JK, T.
6. Design and analysis of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter.
7. Design and analysis of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
8. Design and analysis of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
9. Design and analysis of 4- Bit Multiplier, Divider.
10. Design and analysis of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication and Division.
11. Design and analysis of Finite State Machine.
12. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Semester: 2nd
Subject Name: Digital VLSI Circuit

Course Code: MEC 201 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Issues of Digital IC Design: General overview of design hierarchy, layers of abstraction, integration density and Moore's law, VLSI design styles, packaging styles, design automation principles.	**7**
Unit II	Logic Design: switch logic, gate restoring logic, Programmable Logic Array (PLAs), Finite State Machine (FSM) as a PLA, personality matrix of a PLA, PLA folding, pseudo-nmos logic, BiCMOS logic gates; Basic Circuit Concepts: sheet resistance and area capacitances of layers, driving large capacitive loads, super-buffers, propagation delay models of cascaded pass transistors, wiring capacitances, switching delay in BiCMOS logic circuits; Bipolar ECL.	**8**
Unit III	Inverter : features of ECL gate, robustness and noise immunity, logic design in ECL, single-ended and differential ECL gates; Dynamic CMOS design : steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, np-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme, different logic families like CPL, DCVSL etc.	**9**
Unit IV	Sequential CMOS Logic Circuits: basic regenerative circuits, digital phase-locked loop (DPLL); Low-power CMOS Logic Circuits: low-power design through voltage scaling, estimation and optimization of switching activity, reduction of switched capacitance, adiabatic logic circuits; Subsystem Design: design of arithmetic building blocks like adders and multipliers, barrel and logarithmic shifters, area-time tradeoff, power consumption issues.	**9**
Unit V	Semiconductor Memories : Dynamic Random Access Memories (DRAM), Static RAM, non-volatile memories, flash memories, low-power memory; Case Study *(instructor may choose any suitable digital system; in the following, an example is suggested)* : A RISC Processor - Instruction Set, Pipeline Architecture, Major Logic Blocks, Layout, Functional Verification.	**7**

Text Book:

1- Digital Integrated Circuits. Sung-Mo Kang, Yusuf Leblebici. Tata McGraw-Hill
2- - Digital Integrated Circuits VLSI-Rabaey - Digital Integrated Circuits.

Ram. Deepak

Semester: 2nd

Subject Name: Advance Microprocessor & Microcontroller

Course Code: MEC 202 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Basics of 8085 Microprocessor, architecture and its Memory management. **Introduction to 8086 microprocessor:** Architecture of 8086 (Pin diagram, Functional block diagram, Register organization Arithmetic operations, Logic Operations, Branch operation.	**7**
Unit II	Program structure of 8086, 8086 instruction, Assembler Directives, string, procedures & macros, 8086 interrupts and interrupt applications, Interfacing.	**9**
Unit III	Microcomputer system peripherals, Introduction of 80386 microprocessors, scheduling, memory management, mode of operation, call gate, privilege levels, Interrupt and Exception handling, Paging, introduction to Pentium Processors.	**7**
Unit IV	INTEL 8051 architecture, instruction set and programming, Memory mapping, addressing modes, Registers, expanded modes. Interrupt handling timing and serial I/O. Design and application of Micro-Controller in Data acquisition, Embedded controllers, Process control etc.	**9**
Unit V	**Programming techniques in C:** looping, counting and indexing, Programmable peripheral interface, interfacing keyboard and seven segment display and other output devices, 8051 serial port programming.	**8**

Text and Reference Books:

1. Douglas V Hall "Microprocessors and interfacing" TMH Publication.
2. Muhammad Ali Mazidi "The 8051Microcontroller and Embedded System" TMH Publication.

Semester: 2nd

Subject Name: Advanced VLSI LAB

Course Code: MEC 251 **L T P C**
0 0 4 2

1. Design the following circuits with given specifications*, completing the
   - **a.** Design flow mentioned below:
   - **b.** Draw the schematic and verify the following
     - i) DC Analysis
     - ii) AC Analysis
     - iii) Transient Analysis
   - **c.** Draw the Layout and verify the DRC, ERC
   - **d.** Check for LVS
   - **e.** Extract RC and back annotate the same and verify the Design
2. A Single Stage differential amplifier
   - i) Common source and Common Drain amplifier
3. Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
   - **a.** Draw the schematic and verify the following
     - i) DC Analysis
     - ii) AC Analysis
     - iii) Transient Analysis
   - **b.** Draw the Layout and verify the DRC, ERC
   - **c.** Check for LVS
   - **d.** Extract RC and back annotate the same and verify the Design.
4. Design a comparator with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
   - **a.** Draw the schematic and verify the following
     - i) DC Analysis
     - ii) AC Analysis
     - iii) Transient Analysis
   - **b.** Draw the Layout and verify the DRC, ERC
   - **c.** Check for LVS
   - **d.** Extract RC and back annotate the same and verify the Design.
5. Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library**.
   - **a.** Draw the schematic and verify the following
     - i) DC Analysis
     - ii) AC Analysis
     - iii) Transient Analysis
   - **b.** Draw the Layout and verify the DRC, ERC
   - **c.** Check for LVS
   - **d.** Extract RC and back annotate the same and verify the Design.
6. For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verifies the functionality by completing ASIC Design FLOW.

Semester: 2nd

Subject Name: Advanced Microprocessor & Microcontroller LAB

Course Code: MEC 252

L T P C
0 0 4 2

Experiments Based on Microprocessor (8086/8088)

Assembling and Executing the Program

1. Programs on Data Transfer Instructions.
2. Programs on Arithmetic and Logical Instructions.
3. Programs on Branch Instructions.
4. Programs on Subroutines.
5. Sorting of an Array.
6. Programs on Interrupts (Software and Hardware).
7. 8086 Programs using DOS and BIOS Interrupts.

Experiments Based on Interfacing & Microcontroller (8051)

8. DAC Interface Waveform generations.
9. Stepper Motor Control.
10. Keyboard Interface / LCD Interface.
11. Data Transfer between two PCs using RS.232 C Serial Port.
12. Programs on Data Transfer Instructions using 8051 Microcontroller.
13. Programs on Arithmetic and Logical Instructions using 8051 Microcontroller.
14. Applications with Microcontroller 8051.

Departmental Elective I*

1. MEC 011 - Advance Data Communication Network
2. MEC 012 - Switching Theory and Logic Design
3. MEC 013 - Advance Signal Processing
4. MEC 014 - Fault Tolerant Digital Design

Departmental Elective I

Semester: 2nd

Subject Name: Advanced Data Communication Network

Course Code: MEC 011 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**Introduction to Data Communication and Networks**: Data Communication, Networks, Physical structures, And different topologies, Categories of Networks: LAN, MAN, WAN, Interconnection of networks, The Internet, Protocols and Standards, Standards Organizations. Network Models, Layered tasks, The OSI model, different layers in OSI model. TCP/IP protocol suite ; Line Coding Scheme	**7**
Unit II	**Physical Layer:** Multiplexing, Frequency Division, Wavelength Division, Circuit Switched Networks, Datagram Networks, Virtual Circuit Networks, Structure of a switch, Ethernet Physical Layer,, HDLC, Point to Point Protocol.	**8**
Unit III	**Data Link Layer**: Introduction Types of Errors, Redundancy, Detection Vs Correction, Forward Error Correction Vs Retransmission, Block Coding Error Detection, Error Correction, Hamming Distance, Minimum Hamming Distance .Linear Block Codes, Cyclic Codes Cyclic Redundancy Check, Cyclic Code Analysis, Advantages. Checksum, Framing Fixed and Variable Size Flow and Error Control, Protocols, Noiseless Channels, Simplest and Stop and Wait Protocols. Noisy Channels, Stop and Wait Automatic Repeat Request, Go Back N Automatic Repeat Request, Selective Repeat Automatic Repeat Request. HDLC, Point to Point Protocol.	**7**
Unit IV	**Medium Access**: Random Access ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). Controlled Access Reservation, Polling, Token Passing. Channelization Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA). IEEE Standards, Standard Ethernet, Changes in the Standard, Fast Ethernet, Gigabit Ethernet, IEEE 802.11Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer. Bluetooth Architecture, Radio Layer, Baseband Layer, L2CAP.	**10**
Unit V	**Connecting LANs**: Connecting Devices Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layers Switches, Three Layer Switches, Gateway. Network layer logical addressing. IPv4AddressesAddress Space, Notation, Classful Addressing, Classless Addressing, IPv6 Addresses Structure and Address Space. Internetworking Need For Network Layer, IPv4Datagram,Fragmentation, Routing Delivery forwarding techniques and processes, routing table, Unicast routing, Multicast routing, Transport Layer Protocol : UDP and TCP, ATM, Cryptography, Network Security	**8**

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Text Books:

1. B. A. Forouzan, "Data Communications and Networking", MGH, 4th ed.

Reference Books:

1. A. S. Tanenbaum, "Computer Networks", PHI.
2. W. Stallings, "Data and Computer Communication", PHI.

Semester: 2nd

Subject Name: Switching Theory and Logic Design

Course Code: MEC 012 **L T P C**

3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Vector switching algebra and Vector switching functions. Special class of switching functions: Threshold, Symmetric functions. Functions with decomposable properties, majority and monotonic functions. Logical completeness of switching functions and complete set of logic primitives.	**9**
Unit2	Hazards in combinational circuits and hazard free realization. Boolean differential calculus: Computation of Boolean derivatives and differentials.	**7**
Unit 3	**SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN:** Analysis of clocked synchronous sequential circuits, Moore/Mealy State diagrams, State Table, State Reduction and Assignment, Design of synchronous sequential circuits. **ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN:** Analysis of asynchronous sequential circuit, Cycles Races, Static, Dynamic and Essential hazards, Primitive Flow Table, State Reductions and State Assignment, Design of asynchronous sequential circuits.	**8**
Unit 4	Fault detection and location in combinational circuits: Tabular, ENF, Path Sensitizing and Boolean Difference methods.	**8**
Unit 5	Sequential machines: Initial uncertainty, successor tree and terminal nodes. Homing, distinguishing and synchronizing sequences Identifications of Sequential machines, checking experiments, Special classes of Sequential machines, Information lossless machine, definitely diagnosable machine and linear sequential circuits.	**8**

Text Books:

1. Switching and Finite Automata Theory by Zvi Kohavi and Niraj K. Jha, Tata Mc Graw Hill.
2. Digital circuits and logic design, Samuel C. Lee, PHI.
3. William I. Fletcher," An Engineering Approach to Digital Design", Prentice Hall India.
4. Hill & Peterson, "Switching Circuit & Logic Design", Wiley.

Reference Books:

1. Charles H. Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004.
2. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001.

Semester: 2nd

Subject Name: Advanced Signal Processing

Course Code: MEC 013 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**Review of Discrete time signals:** sequences, representation. Discrete time systems: linear, time in variant, LTI systems, properties, and constant coefficients difference equations. Frequency Domain representation of discrete time signals and systems.	**7**
Unit II	**Review of Z Transform** –Properties, ROC, Stability, Causality, Criterion. Inverse Z Transform, Recursive and Non Recursive systems, Realization of discrete time system.	**8**
Unit III	**Discrete Fourier Transforms:** Definitions, Properties of the DFT, Circular Convolution, Linear Convolution Discrete Cosine Transform, Relationship between DFT and DCT. Computation of DFT: FFT/Decimation in Time and Decimation in Frequency.	**7**
Unit IV	**Finite Impulse Response Filter Design:** Windowing and the Rectangular Window, Other Commonly Used Windows, Examples of Filter Designs Using Windows, The Kaiser Window Application of MATLAB for Design of Digital filter. Effect of Finite register length in filter Design.	**8**
Unit V	**Discrete time Random signals:** Discrete time random process, Averages, Spectrum Representation of finite energy signals, response of linear systems to random signals. Power spectrum estimation: Basic principles of spectrum estimation, estimate of auto con variance, power spectrum, cross con variance and cross spectrum. **Advance signal processing technique and transforms:** multi rate signal processing down sampling/up sampling, introduction to discrete Hilberts Transform, Wavelet Transform, Haar Transform etc.	**10**

Text /Reference Books:

1. Discrete time signal processing by Openheim & Schaffer PHI 2nd Edition.
2. Digital Signal Processing using MATLAB by S. Mitra.
3. Digital Signal Processing By Proakis Pearson Education.

Semester: 2nd

Subject Name: Fault Tolerant Digital Design

Course Code: MEC 014 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**Basic Concept of Reliability:** Definition, Failure Rate, Relation between Mean time and Reliability, Maintainability, Availability, Series and Parallel System. **Faults in Digital Circuits:** Failures and Faults, Modeling of Faults- (Stuck at Faults, Bridging Faults, Stuck Open Faults), Temporary Faults.	8
Unit 2	**Test Generation:** Fault Diagnosis of Digital Systems, Test Generation for Combinational Logic Circuits (One Dimension Path Sensitization, Boolean Difference, D- Algorithm, PODEM), Detection of Multiple Faults in Combinational Logic Circuits, Test Generation for Sequential Logic Circuits, Random Testing, Transition Count Testing, Signature Analysis.	8
Unit 3	**Fault Tolerant Design of Digital System:** Concept of Fault Tolerance, Static Redundancy, Dynamic Redundancy, Hybrid Redundancy, Self Purging Redundancy, Shift out Modular Redundancy, 5MR Reconfiguration Scheme, Fault Tolerant Design of Memory Systems using Error correcting codes, Time Redundancy, Software Redundancy, Fail Soft Operation, Fault Tolerant chip for Design of VLSI Chips.	8
Unit 4	**Self Checking and Fail Safe Logic:** Design of Totally Self Checking Checkers (Two Rail Checkers, Self Checking checkers for m-out –of – n Codes, Self Checking for Burger codes, Low cost residual code), Self Checking sequential Machine, Partially Self Checking Circuits, Fail Safe Design.	8
Unit 5	**Design for Testability:** Testability, Controllability and Observability, Design of Testable Combinational Logic Circuits, Testable Design of Sequential Circuits, Scan Path Techniques for Testable sequential circuits design, Level Sensitive Scan Design, Random Access Scan Techniques, Built in Test, Design Testability into Logic Boards.	8

Text Books:

1. Fault Tolerant and Fault Testable Hardware Design by P. K. Lala , BS publication.
2. Digital circuits and logic design, Samuel C. Lee, by PHI.
3. Diraj K. Pradhan, "Fault Tolerant Computer System Design", Prentice Hall.

Reference Books:

1. M. Abramovici, M.A. Breuer, A.D. Friedman, "Digital systems testing and testable design", Jaico Publishing House.

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Departmental Elective II

1. MEC 021 - Artificial Neural Network
2. MEC 022 - Design Of Digital IC
3. MEC 023 - Micro-controller based system design
4. MEC 024 - Advance Computer Architecture
5. MEC 025 - Pattern Recognition
6. MEC 026 - Compound Semiconductors

Departmental Elective III

1. MEC 031 - Nano Technology
2. MEC 032 - Memory Technologies
3. MEC 033 - CAD of VLSI Design
4. MEC 034 - Artificial Intelligence
5. MEC 035 - Micro Electro Mechanical System
6. MEC 036 - Information Security

Departmental Elective II

Semester: 3rd
Subject Name: Artificial Neural Network

Course Code: MEC 021 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit 1	Introduction: Biological Neural Networks, Characteristics of Neural Networks, Models of Neuron, Basic Learning Rules, Stability & Convergence. Supervised Learning Neural Networks, Adaptive networks, Adaline and madaline, Single layer and multi layer perceptrons Radial basis function networks, Modular neural networks.	**9**
Unit 2	Feedback Neural Networks, Analysis of linear auto adaptive feed forward networks, Analysis of pattern storage Networks, Stochastic Networks & Stimulated Annealing, Boltzman machine. Unsupervised Learning Networks, Competitive learning, Kohonen self-organizing maps, learning vector quantization Principal component analysis of Hebbian Learning, Adaptive Resonance Theory.	**10**
Unit 3	Architectures for Pattern Recognition, Associative memory, Pattern mapping, Stability – Plasticity dilemma, ART, temporal patterns, Pattern visibility: Neocognitron.	**7**
Unit 4	Applications of Neural Networks, Pattern classification, Associative memories, Optimization, Applications in Image Processing, Applications in decision making	**7**
Unit 5	Fuzzy Set Theory Introduction to Fuzzy Set with Properties, Fuzzy Relations, Fuzzy Arithmetic, Fuzzy Logic, Applications and Fuzzy Control.	**7**

Text Books:

1. B. Yegnanarayana, "Artificial Neural Networks", PHI.
2. James A Freeman, David M Skapura, "Neural Networks-Algorithm s, Applications and Programming Techniques," Person Education.
3. S. N. Sivanandam, S. Sumathi, S. N. Deepa, "Introduction to Neural Networks Using MATLAB 6.0" TMH Publication.

Semester: 3rd
Subject Name: Design of Digital IC

Course Code: MEC 022

L T P C
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Basic Electrical Properties of MOS circuits: MOS transistor operation in linear and saturated regions, MOS transistor threshold voltage, MOS switch and inverter, latch-up in CMOS inverter; sheet resistance and area capacitances of layers, wiring capacitances;	**7**
Unit II	CMOS inverter properties - robustness, dynamic performance, regenerative property, inverter delay times, switching power dissipation, Combinational logic design in CMOS	**8**
Unit III	MOSFET scaling - constant-voltage and constant-field scaling; dynamic CMOS design: steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, NP-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme;	**8**
Unit IV	Subsystem design: design of arithmetic building blocks like adders - static, dynamic, Manchester carry-chain, look-ahead, linear and square-root carry-select, carry bypass and pipelined adders and multipliers - serial-parallel Braun, Baugh-Wooley and systolic array multipliers, barrel and logarithmic shifters, area-time tradeoff, power consumption issues;.	**7**
Unit V	Designing semiconductor memory and array structures: memory core and memory peripheral circuitry. Virtual and high speed memory design. Custom cell based design. Digital circuit testing and testability	**10**

Text Books:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation" John Wiley & Sons.

Reference Books:

2. U. Meyer -Baese, "Digital Signal Processing with Field Programmable Gate Arrays" Springer.

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Semester: 3rd

Subject Name: Micro-Controller Based System Design

Course Code: MEC 023 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Various logic families, features, comparison, PLA, PAL, GAL, comparison, combinational PAL, PAL with flip-flops, study of 16L8, 22V10 GAL, dual port RAM, FIFO, FPGA, and Gate Arrays.	**6**
Unit II	Embedded C compiler, advantages, memory models, interrupt functions, code optimization, 89C2051 micro-controller- architecture, comparison with 89C51, design of a simple trainer circuit using 89C51/89C2051 µC, interfacing of DIP switch, LED, 7 segment display, alphanumeric LCD, relay interface, design of a traffic light control system, interfacing programs using C and assembly language.	**8**
Unit III	Analog to digital converters, single slope, dual slope, successive approximation, sigma delta, flash, comparison, typical ICs, A/D interface, digital to analog converters, different types, D/A interface, optically isolated triac interface, design of a temperature control system, interfacing programs using C and assembly language.	**8**
Unit IV	Serial bus standards, I2C bus, SPI bus, operation, timing diagrams, 2 wire serial EEPROM, 24C04, 3wire serial EEPROM, 93C46, interfacing, serial communication standards, RS232, RS422, RS485, comparison, MAX232 line driver/ receiver , interfacing, interfacing programs using C and assembly language, low voltage differential signaling, PC printer port, registers, interfacing, universal serial bus, PCI bus.	**9**
Unit V	Matrix key board interface, AT keyboard, commands, keyboard response codes, watch dog timers, DS1232 watch dog timer, real time clocks, DS1302 RTC, interfacing ,measurement of frequency, phase angle, power factor, stepper motor interface, dc motor speed control, L293 motor driver, design of a position control system, interfacing programs using C and assembly language.	**9**

Text/Reference Books:

1. The 8051 Microcontroller: Muhammad Ali Mazidi, Pearson Education.
2. The 8051 Microcontroller: Kenneth J Ayala, Penram International.
3. Digital fundamentals: Floyd, Pearson Education.
4. Programming and customizing the 8051 µC: Myke Predko, TMH.
5. Programming with ANSI C and turbo C: Kamthane, Pearson Education.
6. Microcomputers and Microprocessors: John Uffenbeck, PHI

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Semester: 3rd

Subject Name: Advance Computer Architecture

Course Code: MEC 024 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Instruction level parallelism ILP- Concepts and challenges, Hardware and software approaches, Dynamic scheduling, Speculation Compiler techniques for exposing ILP, Branch prediction.	**7**
Unit II	Multiple issue processors vliw & epic, Advanced compiler support, Hardware support for exposing parallelism, Hardware versus software speculation mechanisms, IA 64 and Itanium processors, Limits on ILP.	**8**
Unit III	Multiprocessors and thread level parallelism Symmetric and distributed shared memory architectures, performance issues synchronization, models of memory consistency, introduction to multithreading.	**9**
Unit IV	Memory and i/o Cache performance, Reducing cache miss penalty and miss rate, Reducing hit time Main memory and performance, Memory technology. Types of storage devices, Buses, RAID, Reliability, availability and dependability, I/O performance measures, Designing an I/O system.	**8**
Unit V	Multi-core architectures, Software and hardware multithreading, SMT and CMP architectures, Design issues, Case studies, Intel Multi-core architecture, SUN CMP architecture, heterogeneous, multi-core processors , case study: IBM Cell Processor.	**8**

Text Books:

1. John L. Hennessey and David A. Patterson, "Computer architecture – A quantitative Approach, MK publication Elsevier.

Reference Books:

1. Kai Hwang and Zhi.Wei Xu, "Scalable Parallel Computing", Tata McGraw Hill, T. Cormen, C. Leiserson and R. A. Rivest, Algorithms, MIT Press and McGraw-Hill.
2. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture "A Hardware/ software approach" , Morgan Kaufmann /Elsevier Publishers.

Semester: 3rd
Subject Name: Pattern Recognition

Course Code: MEC 025 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**Introduction:** Basics of pattern recognition, Design principles of pattern recognition system, Learning and adaptation, Pattern recognition approaches, Mathematical foundations – Linear algebra, Probability Theory, Expectation, mean and covariance, Normal distribution, multivariate normal densities, Chi squared test.	**8**
Unit II	**Statistical Patten Recognition:** Bayesian Decision Theory, Classifiers, Normal density and discriminant functions.	**8**
Unit III	**Parameter Estimation Methods:** Maximum-Likelihood estimation, Bayesian Parameter estimation, Dimension reduction methods - Principal Component Analysis (PCA), Fisher Linear discriminant analysis, Expectation-maximization (EM), Hidden Markov Models (HMM), Gaussian mixture models.	**7**
Unit IV	**Nonparametric Techniques:** Density Estimation, Parzen Windows, K-Nearest Neighbor Estimation, Nearest Neighbor Rule, Fuzzy classification.	**10**
Unit V	**Unsupervised Learning & Clustering:** Criterion functions for clustering, Clustering Techniques: Iterative square - error partitional clustering – Kmeans, agglomerative hierarchical clustering, Cluster validation.	**7**

Reference Books:

1. Richard O. Duda, Peter E. Hart and David G. Stork, "Pattern Classification", 2ndEdition, John Wiley, 2006.
2. C. M. Bishop, "Pattern Recognition and Machine Learning", Springer, 2009.
3. S. Theodoridis and K. Koutroumbas, "Pattern Recognition", 4thEdition, Academic Press.

Semester: 3rd

Subject Name: Compound Semiconductors

Course Code: MEC 026 **L T P C**

3 1 0 4

Unit	Topic	No. of Lecture
Unit 1	Structure, bonding and ionicity of compound semiconductors, binary and ternary alloy systems; phase diagrams - Ga-As, InP, CdTe, and HgCdTe systems; stoichiometry and composition of IIIV and II-V compounds, Charge transport, lattice modes and scattering processes, ionized impurity, acoustic, piezoelectric and polar optical scattering, quantum effects - 2 dimensional transport	**10**
Unit 2	quantum hall effect, super lattices, resonant tunneling, transport in presence of magnetic fields, Gunn effect, impact ionization and avalanche breakdown, Optical absorption and emission, band structure, dependence on temperature, pressure, composition and degeneracy, impurity and free carrier absorption.	**9**
Unit 3	electrons at heterojunctions, electrons in nanostructures, electrons in coupled nanostructures, photons	**7**
Unit 4	substrates and epitaxy, thin films, device processing, electronics, in-plane optoelectronics, out-of-plane optoelectronics	**7**
Unit 5	magneto-optical effects, luminescence, heterojunctions and interfaces, growth and process induced defects, deep levels, persistent photoconductivity, Applications of compound semiconductors as sensors and actuators.	**7**

Text Books:

1. World of Compound semiconductor.

Semester: 3rd
Subject Name: Dissertation-I

Course Code: MEC 351

L T P C
0 0 16 12

Students have to perform a mini project work related to their respective stream in M. Tech. The project work may be software or hardware based. /it may be extendable to major project in next semester.

Departmental Elective III

Semester: 3rd
Subject Name: Nano Technology

Course Code: MEC 031 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Introduction, science behind nanotechnology, bio systems, molecular recognition, quantum mechanics & quantum ideas, optics. Smart materials & Sensors, self healing structures	**7**
Unit II	Heterogeneous nano structures & composites, encapsulations, natural nanoscale sensors, electromagnetic sensors, biosensors, electronic noses.	**8**
Unit III	Nanostructures, Micro/Nanodevices, Nanomaterials Synthesis and Applications, Molecule-Based Devices- Introduction to Carbon Nanotubes, Nanowires	**8**
Unit IV	Introduction to Micro/Nanofabrication.- Stamping Techniques. Methods and Applications. Materials Aspects of Micro- and Nanoelectromechanical Systems- MEMS/NEMS Devices and Applications, Nanodevices, Scanning Probe Microscopy	**7**
Unit V	Noncontact Atomic Force Microscopy and Its Related Topics - Low Temperature Scanning Probe Microscopy, Dynamic Force Microscopy- Nanolithography, Lithography using photons, electron beams soft lithography, Bio- medical applications.	**10**

Text/Reference Books:

1. Mark Ratner, Daniel Rattner, "Nanotechnology: A Gentle Introduction to the Next Big Idea", Pearson Education.
2. Nanotechnology :Principals &practices, Sulbha K. Kulkarni, Capital publishing company, ISBN:-
   81-85589-29-1.

Semester: 3rd
Subject Name: Memory Technologies

Course Code: MEC 032 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs.	**7**
Unit II	DRAMs, DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP.	**8**
Unit III	EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application.	**9**
Unit IV	Specific Memory Testing. General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.	**8**
Unit V	Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories(MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.	**8**

Text/Reference Books:

1. Ashok K. Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice- Hall of India Private Limited, New Delhi, 1997.
2. Manish Verma and Peter Marwedel "Advance Memory optimization techniques for Low Power Embedded processors", Springer Publication.
3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

Semester: 3rd
Subject Name: CAD of VLSI Design

Course Code: MEC 033

L T P C
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**VLSI DESIGN METHODOLOGIES:** Introduction to VLSI Design methodologies, Review of Data structures and algorithms, Review of VLSI Design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, general purpose methods for combinatorial optimization.	**8**
Unit II	**DESIGN RULES:** Layout Compaction, Design rules, problem formulation, algorithms for constraint graph compaction, placement and partitioning, Circuit representation, Placement algorithms, partitioning	**8**
Unit III	**FLOOR PLANNING:** Floor planning concepts, shape functions and floor-plan sizing, Types of local routing problems, Area routing, channel routing, global routing, algorithms for global routing.	**7**
Unit IV	**SIMULATION:** Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.	**9**
Unit V	**MODELLING AND SYNTHESIS:** High level Synthesis, Hardware models, Internal representation, Allocation assignment and scheduling, Simple scheduling algorithm, Assignment problem, High level transformations.	**8**

Text Books:

1. K. Hoffman and R.E. Kunze, Linear Algebra, Prentice Hall (India).

Reference Books:

1. N. Balabanian and T.A. Bickart, Linear Network Theory: Analysis, Properties, Design and Synthesis, Matrix Publishers.
2. T. Cormen, C. Leiserson and R. A. Rivest, Algorithms, MIT Press and McGraw-Hill.

Semester: 3rd
Subject Name: Artificial Intelligence

Course Code: MEC 034 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit 1	Introduction to Artificial Intelligence Definition, AI Applications, AI representations, properties of internal representations Heuristic Search Techniques, Best File Search, Mean and End Analysis, A* and AO* Algorithms.	**9**
Unit 2	Neural Networks, Learning by training neural networks, Introduction to neural net works, Neural net architecture & applications, Natural language processing & understanding & paragmatic, Syntactic, Semantic, Qualities, finite state machines, RTN, ATN, understanding sentences.	**8**
Unit 3	Game Playing & Predicate Logic Minimax search procedure, Alpha-beta cut-offs, Waiting for Quiescence, Secondary Search, Predicate Calculus, Predicate and arguments, ISA Hierarchy, Frame Notation, Resolution, Natural Deduction.	**8**
Unit 4	Knowledge Representation Using Non-Monotonic Logic Truth Maintenance System, Statistical and Probabilistic Reasoning, Semantic-net Frames, Script, Conceptual Dependency.	**7**
Unit 5	Planning Block world, strips, Implementation using goal stack, Non-linear planning using goal stacks, Hierarchical planning, List commitment strategy. Expert Systems Utilization and functionality, Architecture of expert systems, Knowledge representation, Two case studies on expert systems.	**8**

Reference Books/Text Books:

1. Ela Kumar, "Artificial Intelligence" I. K. International.
2. Rajendra Akerkar, "Introduction to Artificial Intelligence" PHI
3. K. Uma Rao, "Artificial Intelligence and Neural Network", Pearson Publication
4. Eugane. Charniak, Drew McDermott, "Introduction to Artificial Intelligence", Pearson Education.
5. Kishan Mehrotra, Sanjay Rawika, K. Mohan, "Artificial Neural Network" .
6. Rajendra Akerkar, "Introduction to Artificial Intelligence", Prentice Hall Publication.
7. S. N. Sivanandam, S. Sumathi, S. N. Deepa, "Introduction to Neural Networks Using MATLAB" TMH Publication.

Semester: 3rd

Subject Name: Micro Electro Mechanical System

Course Code: MEC 035 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit 1	**INTRODUCTION TO MICROSYSTEMS:** Review of microelectronics manufacture and introduction to MEMS Overview of Microsystems technology. Laws of scaling. The multi disciplinary nature of MEMS. Survey of materials central to micro engineering. Applications of MEMS in various industries.	**9**
Unit 2	**MICRO MANUFACTURING TECHNIQUES:** Photolithography, Film deposition, Etching processes, Bulk micro machining, silicon surface micro machining, LIGA process, Rapid micro product development.	**8**
Unit 3	**MICRO SENSORS AND MICRO ACTUATORS:** Energy conversion and force generation, Electromagnetic Actuators, Reluctance motors, piezoelectric actuators, bi-metal-actuator Friction and wear. Transducer principles, Signal detection and signal processing, Mechanical and physical sensors, Acceleration sensor, pressure sensor, Sensor arrays.	**9**
Unit 4	**INTRODUCTION TO MICRO / NANO FLUIDS:** Fundamentals of micro fluidics, Micro pump – introduction – Types – Mechanical Micro pump – Non Mechanical micro pumps, Actuating Principles, Design rules for micro pump – modeling and Simulation , Verification and testing – Applications.	**7**
Unit 5	**MICROSYSTEMS DESIGN AND PACKAGING:** Design considerations, Mechanical Design, Process design, Realization of MEMS components using intellisuite. Micro system packaging, Packing Technologies, Assembly of Microsystems, Reliability in MEMS.	**7**

Text Books:

1. Mohamed Gad – el – Hak , MEMS Handbook, CRC Press, 2002.
2. Rai-Choudhury P. MEMS and MOEMS Technology and Applications, PHI Learning Private Limited, 2009.

Reference Books:

1. Sabrie Solomon, Sensors Handbook, Mc Graw Hill, 1998.
2. Marc F Madou, Fundamentals of Micro Fabrication, CRC Press, 2nd Edition, 2002.
3. Francis E.H. Tay and W.O. Choong , Micro fluidics and Bio mems application, IEEE Press New York, 1997.
4. Trimmer William S., Ed., Micromachanics and MEMS, IEEE Press New York, 1997.
5. Maluf, Nadim, An introduction to Micro electro mechanical Systems Engineering, AR Tech house, Boston 2000.

Semester: 3rd
Subject Name: Information Security

Course Code: MEC 036 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**Information Security:** Attacks on information, components of Information Security, Cryptographic techniques, public & private key, mathematical tools of cryptography, Cryptography techniques, Authentication access control, Digital signature, Certificates & standards.	**9**
Unit II	**Cypher Algorithm:** Design principles of block ciphers & Block Cipher Algorithms, Electronic mail security, RSA algorithm, MD5, IDEA, RC2, RC5 algorithm, Stenography techniques.	**8**
Unit III	**Web Security:** SSL protocol security, HTTPS, WTLS protocol in WAP, Introduction to Web based bio AuC, issues of s/w piracy & copyright, Introduction to IT act 2000.	**7**
Unit IV	**Mobile Attacks:** 3 GPP security, Mobile Virtual Private n/w, Smart Card security, RFID security, Mobile Agent security, Mobile virus, mobile worms	**8**
Unit V	**Database Security Systems:** Network security concept, Trojans, Intrusion detection, Firewall, Cyber law related to E-commerce.	**8**

Reference Books:

1. Stallings, William- "Cryptography & Network Security: principle and Practices" Pearson Education.
2. Asoke K Talukder, Hasan Ahamad, Roopa R Yavagal "Mobile Computing" TMH Publication.

Semester: 4th
Subject Name: Dissertation-II

Course Code: MEC 451

L T P C
0 0 20 24

A student has to make a latest technology based project in their respective stream. It may be hardware or software based.

Semester: 2nd
Subject Name: Low Power VLSI Design

Course Code: MEC 203 **L T P C**
3 1 0 4

Unit	Topic	No. of Lecture
Unit I	**Introduction to VLSI design:** MOS Physics, Structure and operation of MOSFETs, MOSFET current- voltage characteristics, MOSFET Modeling, MOSFET Scaling, MOSFET Capacitances.	**9**
Unit II	**Low Power Design:** Introduction, Needs of Low power VLSI chips, dynamic power dissipation, short circuit power dissipation, leakage power dissipation.	**8**
Unit III	**MOSFET Scaling: constant** field scaling, constant voltage scaling, limitations on scaling of MOSFET, comparison between constant field and constant voltage scaling, advantages of scaling, disadvantages of scaling.	**7**
Unit IV	**Low–Power CMOS Logic Circuits:** Introduction, Low – Power Design through voltage scaling, Variable threshold CMOS Circuits, Multiple threshold CMOS circuits, Estimation and Optimization of switching activity, Reduction of Switched Capacitance and Adiabatic Logic Circuits. **POWER ESTIMATION:** Power Estimation techniques, logic power estimation, Simulation power analysis, Probabilistic power analysis.	**9**
Unit V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER:** Synthesis for low power – Behavioral level transform – software design for low power.	**7**

Text Books:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer.

Reference Books:

1. J.B. Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley.
2. A.P .Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design" Kluwer.

Rami Deepa